

# EE 330

## Lecture 42

### Digital Circuits

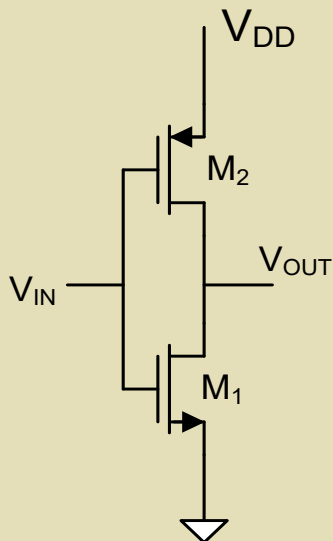
- Propagation Delay with Minimum Sized Gates
- Propagation Delay with Arbitrary Gate Sizing
- Optimally driving large capacitive loads
- Logic Effort Method for Signal Propagation

# Fall 2023 Exam Schedule

<b>Exam 1</b>	<b>Friday Sept 22</b>	
<b>Exam 2</b>	<b>Friday Oct 20</b>	
<b>Exam 3</b>	<b>Friday Nov. 17</b>	
<b>Final</b>	<b>Monday Dec 11</b>	<b>12:00 – 2:00 p.m.</b>

# The Reference Inverter

## Reference Inverter



Assume  $\mu_n/\mu_p=3$

$W_n=W_{MIN}$ ,  $W_p=3W_{MIN}$

$L_n=L_p=L_{MIN}$

In 0.5u proc  $t_{REF}=20ps$ ,

$C_{REF}=4fF$ ,  $R_{PDREF}=R_{PUREF}=2.5K$

$$R_{PDREF} = R_{PUREF}$$

$$C_{REF} = C_{IN} = 4C_{OX} W_{MIN} L_{MIN}$$

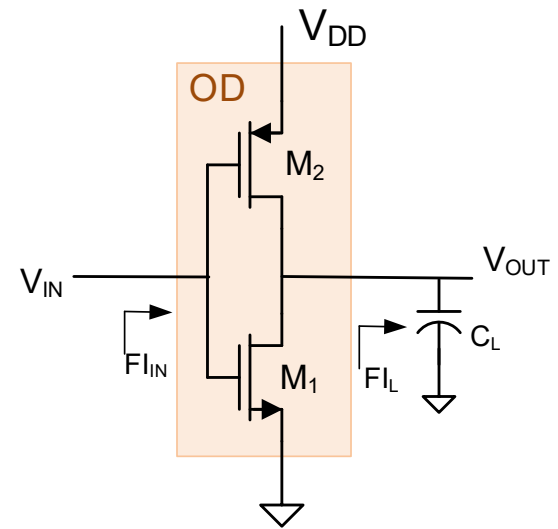
$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} \stackrel{V_{Tn}=.2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})}$$

$$t_{HLREF} = t_{LHREF} = R_{PDREF} C_{REF}$$

$$t_{REF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF}$$

(Note: This  $C_{OX}$  is somewhat larger than that in the 0.5u ON process)

# Overdrive Factors



Scaling widths of ALL devices by constant ( $W_{\text{scaled}} = W \times \text{OD}$ ) will change “drive” capability relative to that of the reference inverter but not change relative value of  $t_{\text{HL}}$  and  $t_{\text{LH}}$

$$R_{\text{PD}} = \frac{L_1}{\mu_n C_{\text{OX}} W_1 (V_{\text{DD}} - V_{\text{Tn}})}$$



$$R_{\text{PDOD}} = \frac{L_1}{\mu_n C_{\text{OX}} [\text{OD} \cdot W_1] (V_{\text{DD}} - V_{\text{Tn}})} = \frac{R_{\text{PD}}}{\text{OD}}$$

$$R_{\text{PU}} = \frac{L_2}{\mu_p C_{\text{OX}} W_2 (V_{\text{DD}} + V_{\text{Tp}})}$$



$$R_{\text{PUOD}} = \frac{L_2}{\mu_p C_{\text{OX}} [\text{OD} \cdot W_2] (V_{\text{DD}} + V_{\text{Tp}})} = \frac{R_{\text{PU}}}{\text{OD}}$$

$$t_{\text{PROP}} = t_{\text{REF}} \cdot \text{FL}_L \cdot \frac{1}{\text{OD}}$$

Scaling widths of ALL devices by constant will change  $\text{FI}_{\text{IN}}$  to gate by OD

$$C_{\text{IN}} = C_{\text{OX}} (W_1 L_1 + W_2 L_2)$$

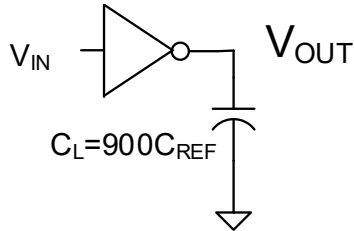


$$C_{\text{INOD}} = C_{\text{OX}} ([\text{OD} \cdot W_1] L_1 + [\text{OD} \cdot W_2] L_2) = \text{OD} \cdot C_{\text{IN}}$$

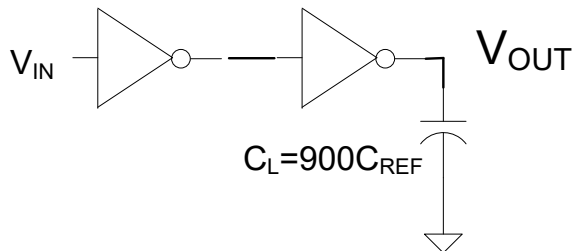
# Propagation Delay with Over-drive Capability

## Example

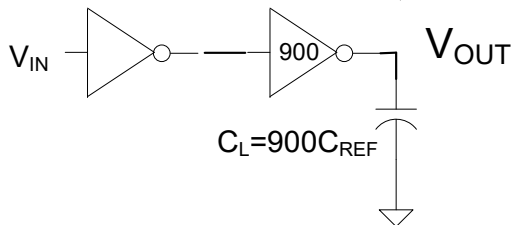
Compare the propagation delays. Assume the OD is 900 in the third case and 30 in the fourth case. Don't worry about the extra inversion at this time.



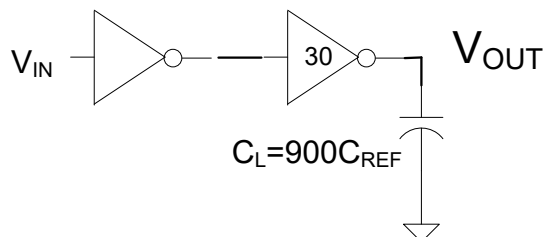
$$t_{PROP} = 900t_{REF}$$



$$t_{PROP} = t_{REF} + 900t_{REF} = 901t_{REF}$$



$$t_{PROP} = 900t_{REF} + t_{REF} = 901t_{REF}$$



$$t_{PROP} = 30t_{REF} + 30t_{REF} = 60t_{REF}$$

- **Dramatic reduction in  $t_{PROP}$  is possible** (input is driving same in all 3 cases)
- **Will later determine what optimal number of stages and sizing is**

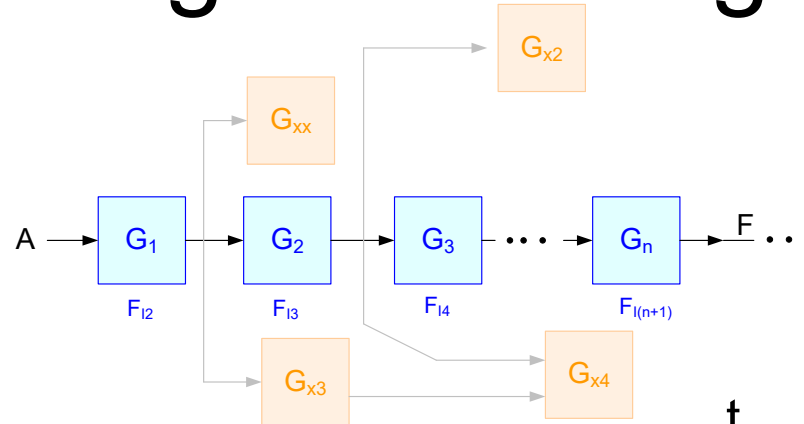
# Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Will consider an example with the five cases*

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
- Combination of equal rise/fall, minimum size and overdrive

*Will develop the analysis methods as needed*

# Propagation Delay in Multiple-Levels of Logic with Stage Loading



- Equal rise/fall (no overdrive)

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n F_{l(k+1)}$$

- Equal rise/fall with overdrive

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n \frac{F_{l(k+1)}}{\text{OD}_k}$$

- Minimum Sized

$$t_{\text{PROP}} = ?$$

- Asymmetric Overdrive

$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{l(k+1)} \left( \frac{1}{\text{OD}_{\text{HLK}}} + \frac{1}{\text{OD}_{\text{LHK}}} \right) \right)$$

- Combination of equal rise/fall, minimum size and overdrive

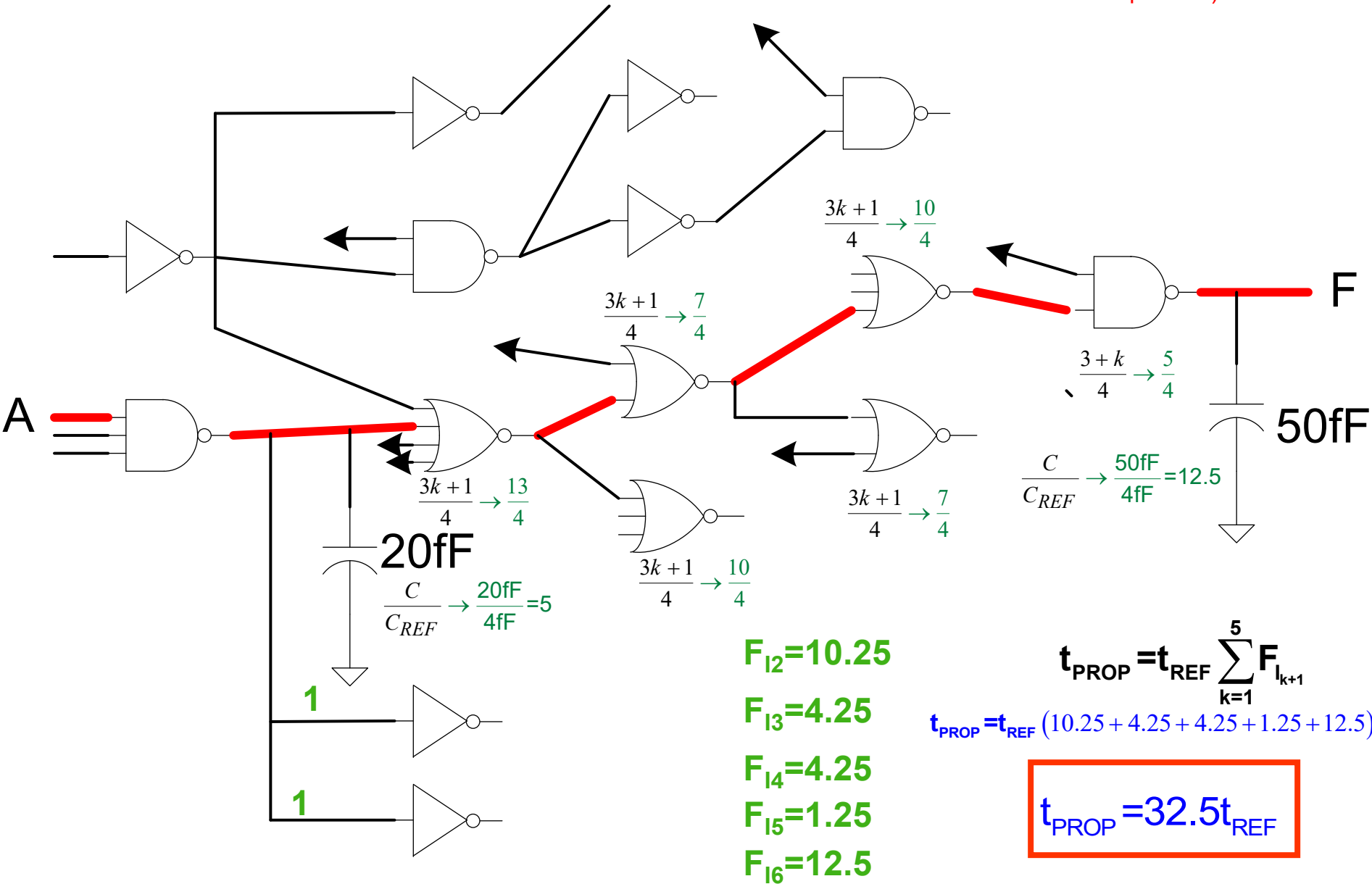
$$t_{\text{PROP}} = ?$$

# Review from Last Time

## Equal rise-fall gates, no overdrive

In 0.5u proc  $t_{REF}=20ps$ ,  
 $C_{REF}=4fF, R_{PDREF}=2.5K$

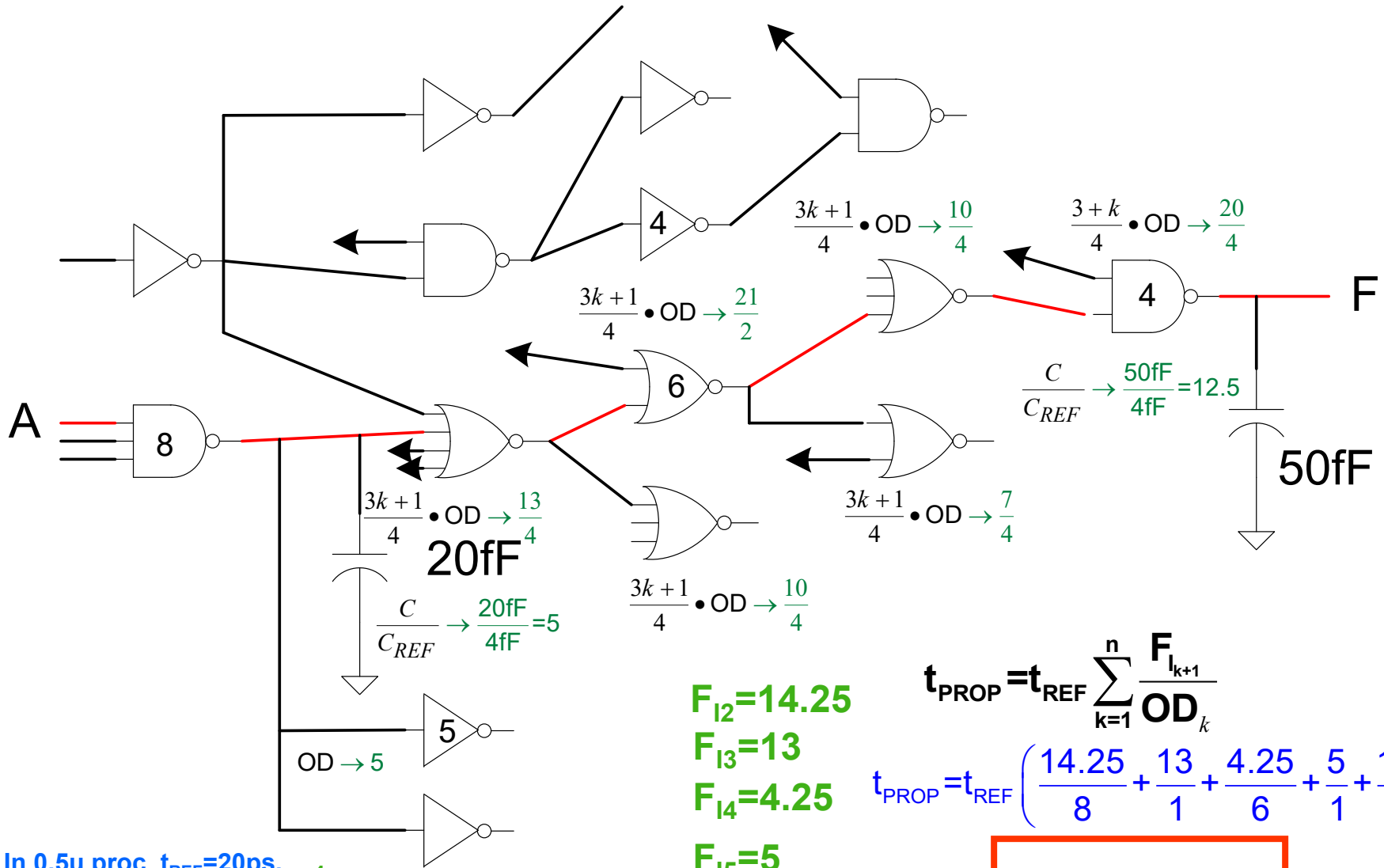
(Note: This  $C_{OX}$  is somewhat larger than that in the 0.5u ON process)





# Review from Last Time

## Equal rise-fall gates, with overdrive



In 0.5u proc  $t_{REF}=20ps$ ,  $C_{REF}=4fF, R_{PDREF}=2.5K$

(Note: This  $C_{OX}$  is somewhat larger than that in the 0.5u ON process)

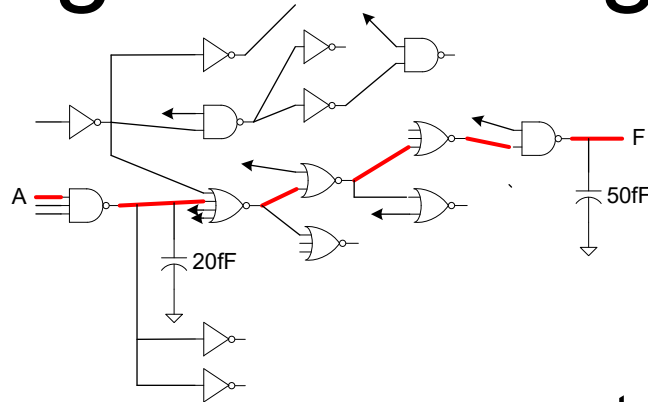
- $F_{12}=14.25$
- $F_{13}=13$
- $F_{14}=4.25$
- $F_{15}=5$
- $F_{16}=12.5$

$$t_{PROP} = t_{REF} \sum_{k=1}^n \frac{F_{l_{k+1}}}{OD_k}$$

$$t_{PROP} = t_{REF} \left( \frac{14.25}{8} + \frac{13}{1} + \frac{4.25}{6} + \frac{5}{1} + \frac{12.5}{4} \right)$$

$$t_{PROP} = 23.6 t_{REF}$$

# Propagation Delay in Multiple-Levels of Logic with Stage Loading



- Equal rise/fall (no overdrive)

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n F_{l(k+1)}$$

- Equal rise/fall with overdrive

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n \frac{F_{l(k+1)}}{\text{OD}_k}$$



- Minimum Sized

$$t_{\text{PROP}} = ?$$

- Asymmetric Overdrive

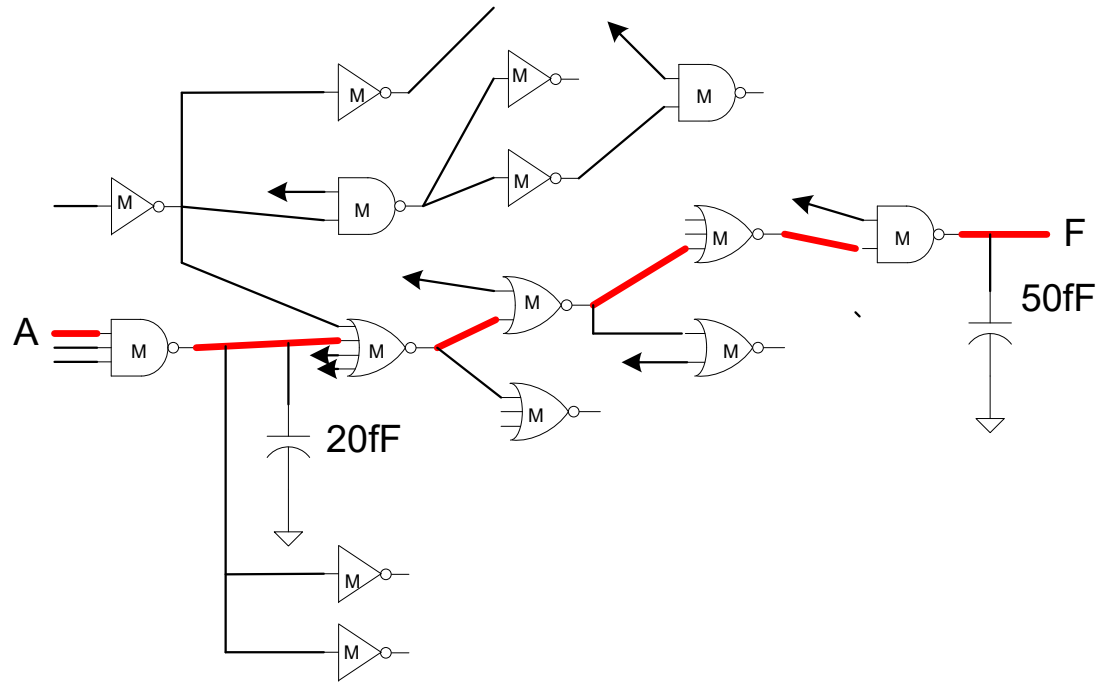
$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{l(k+1)} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right)$$

- Combination of equal rise/fall, minimum size and overdrive

$$t_{\text{PROP}} = ?$$

# Propagation Delay in Multiple-Levels of Logic with Stage Loading

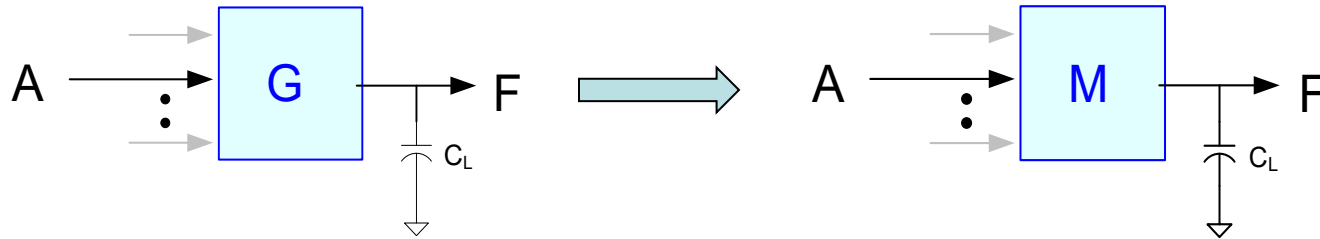
*Minimum-sized gates*



$$t_{\text{PROP}} = t_{\text{REF}} \bullet ?$$

Observe that a minimum-sized gate is simply a gate with asymmetric overdrive

# Propagation Delay with Minimum-Sized Gates



Recall propagation delay for asymmetric overdrive:

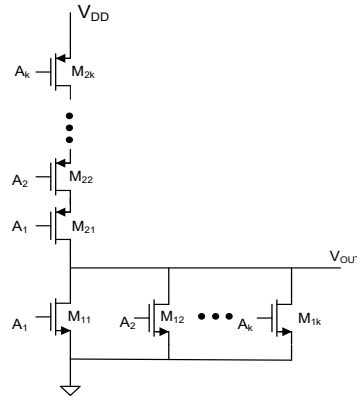
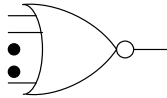
$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{I^{(k+1)}} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right)$$

Thus for minimum-sized devices:

$$\frac{t_{\text{PROP}}}{t_{\text{REF}}} = \left( \frac{1}{2} \sum_{k=1}^n F_{I^{(k+1)}} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right)$$

- Still need  $\text{OD}_{\text{HL}}$  and  $\text{OD}_{\text{LH}}$  for minimum-sized gates
- Still need  $\text{FI}$  for minimum-sized gates

# Propagation Delay with minimum-sized gates

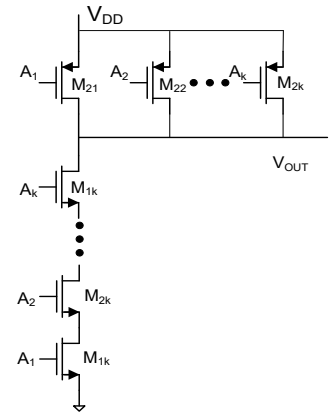
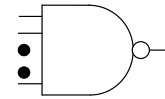


$$OD_{HL}=?$$

$$OD_{HL}=1$$

$$OD_{LH}=?$$

$$OD_{LH}=\frac{1}{3k}$$



$$OD_{HL}=?$$

$$OD_{HL}=1/k$$

$$OD_{LH}=?$$

$$OD_{LH}=\frac{1}{3}$$

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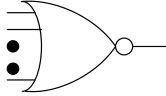
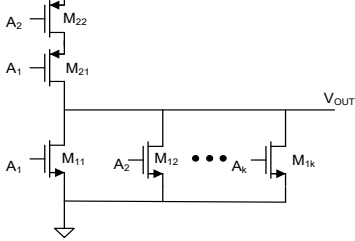
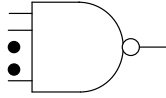
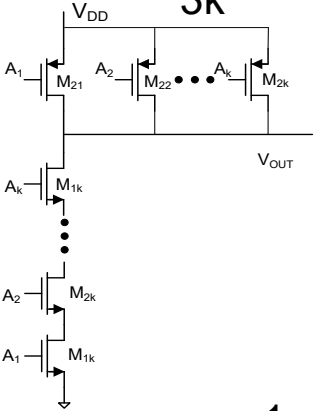

$$FI=2C_{OX}W_{MIN}L_{MIN}$$

$$C_{REF}=4C_{OX}W_{MIN}L_{MIN}$$

$$FI=\frac{C_{REF}}{2}$$

# Propagation Delay in Multiple-Levels of Logic with Stage Loading

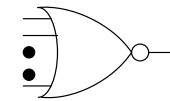
## Minimum-sized gates

	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized		
$C_{IN}/C_{REF}$					
Inverter	1	OD			
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \cdot OD$			
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \cdot OD$		$OD_{HL} = 1$	$OD_{LH} = \frac{1}{3k}$
Overdrive					
Inverter					
HL	1	OD			
LH	1	OD			
NOR					
HL	1	OD			
LH	1	OD			
NAND					
HL	1	OD			
LH	1	OD			
$t_{PROP}/t_{REF}$	$\sum_{k=1}^n F_{l(k+1)}$	$\sum_{k=1}^n \frac{F_{l(k+1)}}{OD_k}$		$OD_{HL} = 1/k$	$OD_{LH} = \frac{1}{3}$
					$F_I = \frac{C_{REF}}{2}$

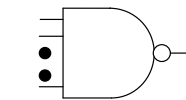
# Propagation Delay in Multiple-Levels of Logic with Stage Loading

## Minimum-sized gates

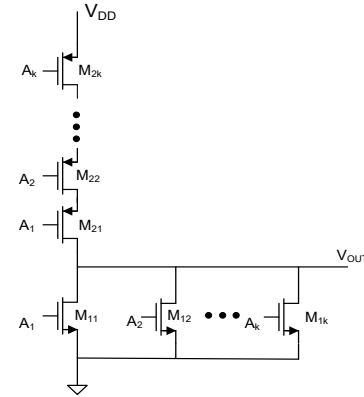
	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized
$C_{IN}/C_{REF}$			
Inverter	1	OD	1/2
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \cdot OD$	1/2
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \cdot OD$	1/2
Overdrive			
Inverter			
HL	1	OD	1
LH	1	OD	1/3
NOR			
HL	1	OD	1
LH	1	OD	1/(3k)
NAND			
HL	1	OD	1/k
LH	1	OD	1/3
$t_{PROP}/t_{REF}$	$\sum_{k=1}^n F_{l(k+1)}$	$\sum_{k=1}^n \frac{F_{l(k+1)}}{OD_k}$	$\frac{1}{2} \sum_{k=1}^n F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$



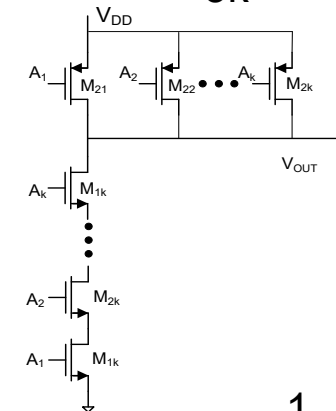
$$OD_{HL} = 1$$



$$OD_{HL} = 1/k$$



$$OD_{LH} = \frac{1}{3k}$$



$$OD_{LH} = \frac{1}{3}$$


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$$FI = \frac{C_{REF}}{2}$$

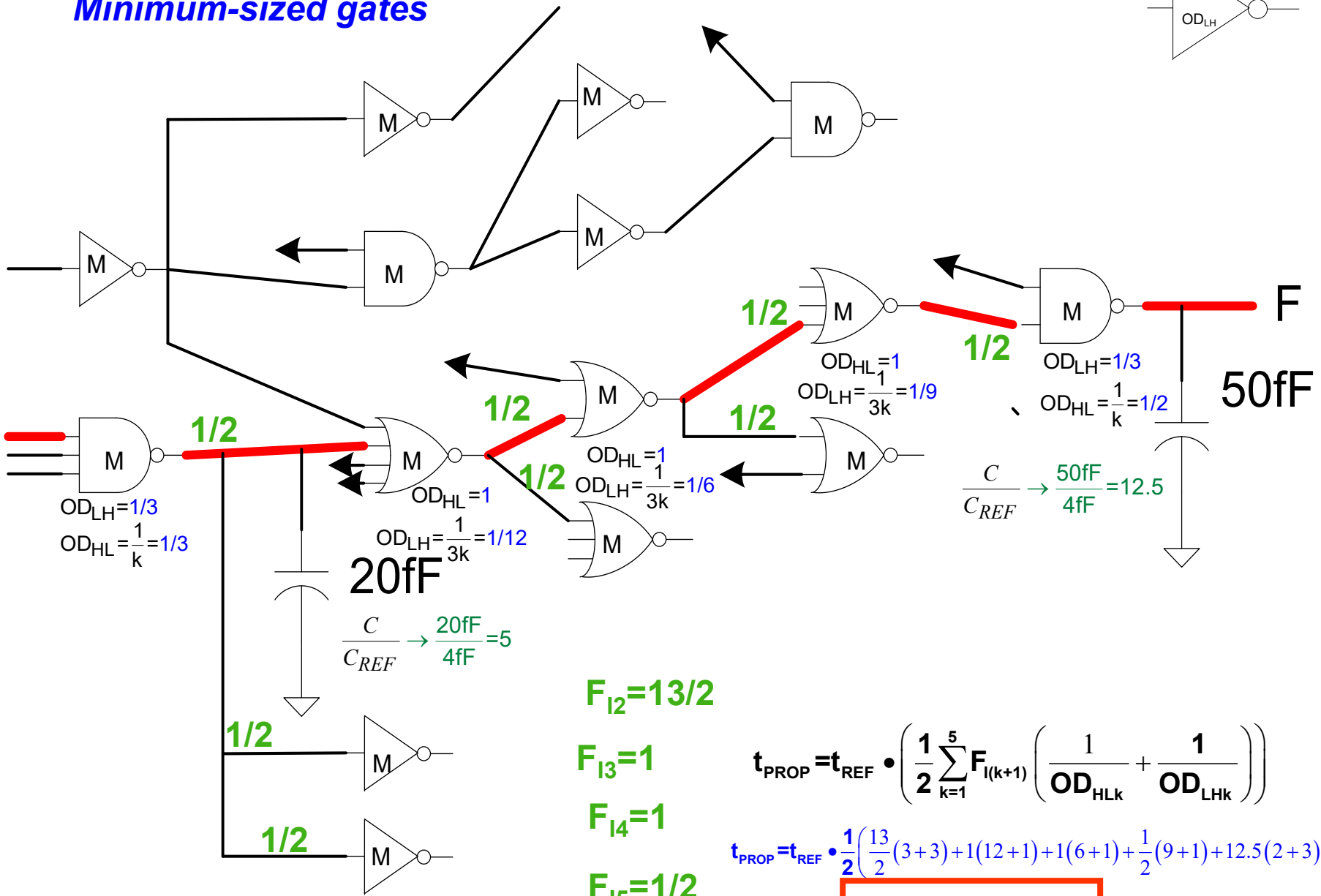
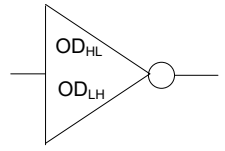
# Propagation Delay in Multiple-Levels of Logic with Stage Loading

## Minimum-sized gates

	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized
$C_{IN}/C_{REF}$			
Inverter	1	OD	1/2
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \cdot OD$	1/2
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \cdot OD$	1/2
Overdrive			
Inverter			
HL	1	OD	1
LH	1	OD	1/3
NOR			
HL	1	OD	1
LH	1	OD	1/(3k)
NAND			
HL	1	OD	1/k
LH	1	OD	1/3
$t_{PROP}/t_{REF}$	$\sum_{k=1}^n F_{l(k+1)}$	$\sum_{k=1}^n \frac{F_{l(k+1)}}{OD_k}$	$\frac{1}{2} \sum_{k=1}^n F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$



# Minimum-sized gates

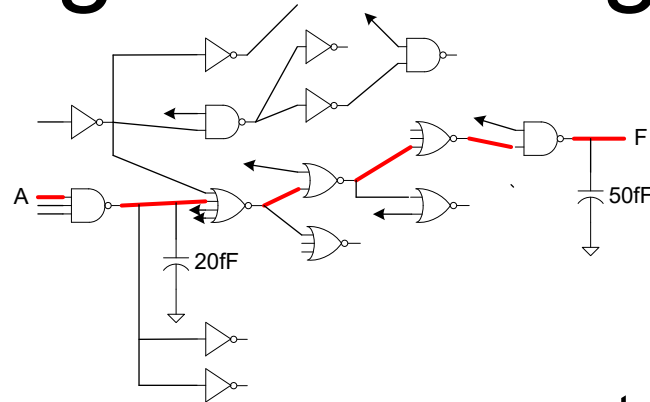


$$t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^5 F_{I(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

$$t_{PROP} = t_{REF} \cdot \frac{1}{2} \left( \frac{13}{2}(3+3) + 1(12+1) + 1(6+1) + \frac{1}{2}(9+1) + 12.5(2+3) \right)$$

$t_{PROP} = 63.25 \cdot t_{REF}$

# Propagation Delay in Multiple-Levels of Logic with Stage Loading



- Equal rise/fall (no overdrive)

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n F_{I_{(k+1)}}$$

- Equal rise/fall with overdrive

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n \frac{F_{I_{(k+1)}}}{\text{OD}_k}$$

- Minimum Sized

$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{I_{(k+1)}} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right)$$



- Asymmetric Overdrive

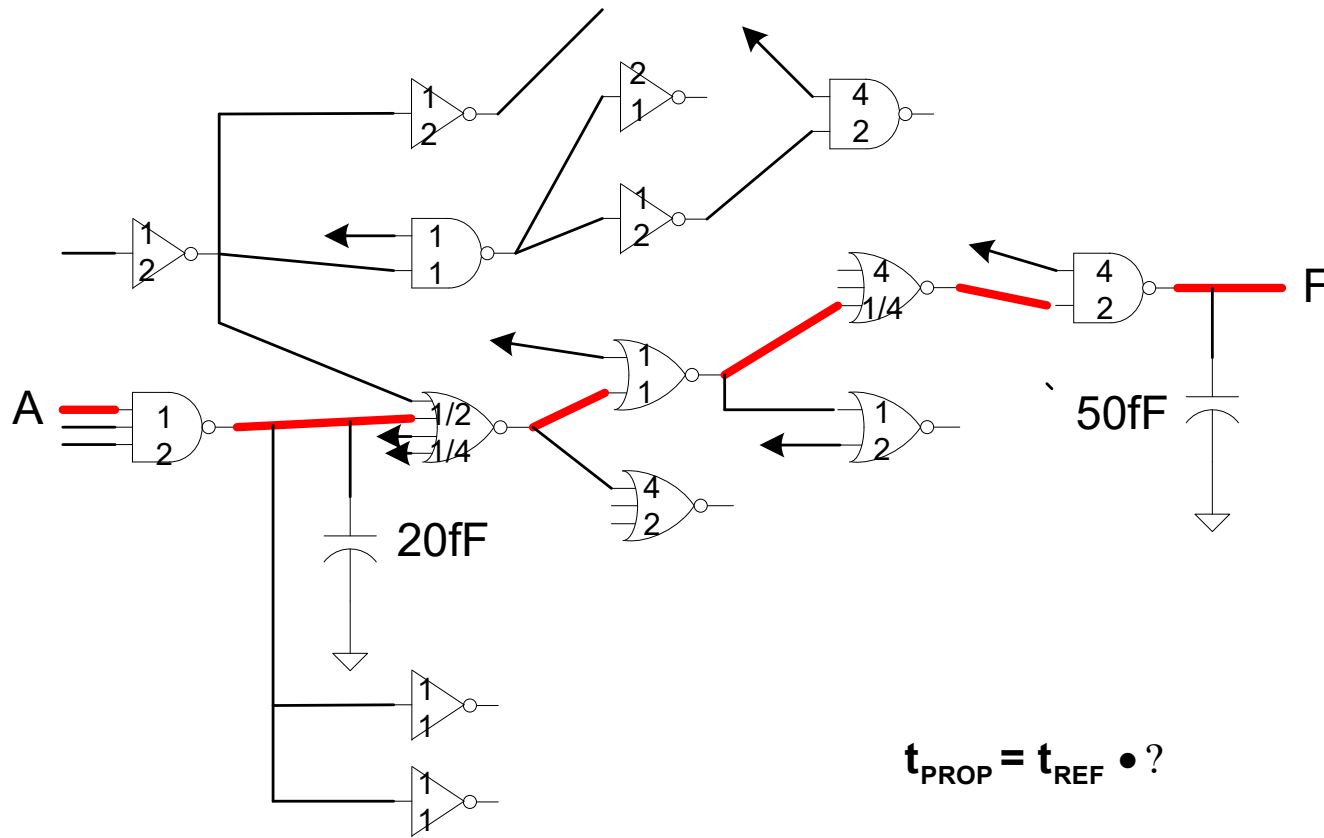
$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{I_{(k+1)}} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right) \checkmark$$

- Combination of equal rise/fall, minimum size and overdrive

$$t_{\text{PROP}} = ?$$

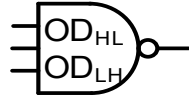
# Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Asymmetric-sized gates*



# Propagation Delay in Multiple-Levels of Logic with Stage Loading

## Asymmetric-sized gates



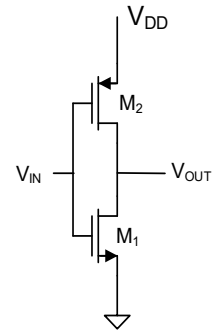
	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD <sub>HL</sub> , OD <sub>LH</sub> )
$C_{IN}/C_{REF}$				
Inverter	1	OD	1/2	?
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \cdot OD$	1/2	?
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \cdot OD$	1/2	?
Overdrive				
Inverter				
HL	1	OD	1	OD <sub>HL</sub>
LH	1	OD	1/3	OD <sub>LH</sub>
NOR				
HL	1	OD	1	OD <sub>HL</sub>
LH	1	OD	1/(3k)	OD <sub>LH</sub>
NAND				
HL	1	OD	1/k	OD <sub>HL</sub>
LH	1	OD	1/3	OD <sub>LH</sub>
$t_{PROP}/t_{REF}$	$\sum_{k=1}^n F_{l(k+1)}$	$\sum_{k=1}^n \frac{F_{l(k+1)}}{OD_k}$	$\frac{1}{2} \sum_{k=1}^n F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$	$\frac{1}{2} \sum_{k=1}^n F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$

$$t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

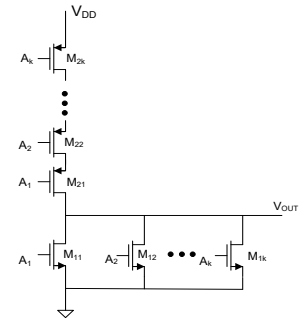
# Asymmetric-sized gates

$$C_{IN}/C_{REF}$$

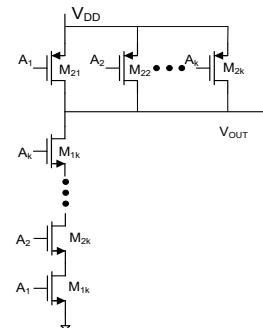
## Inverter



## NOR



## NAND

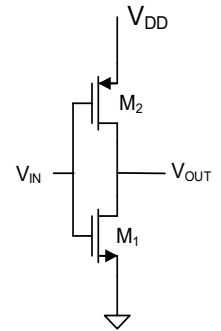


# Asymmetric-sized gates

$$C_{IN}/C_{REF}$$

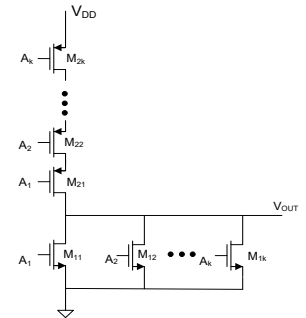
## Inverter

$$\frac{C_{IN}}{C_{REF}} = \frac{C_{OX} W_n OD_{HL} L + C_{OX} (3W_n) OD_{LH} L}{4C_{OX} W_n L} = \frac{OD_{HL} + 3OD_{LH}}{4}$$



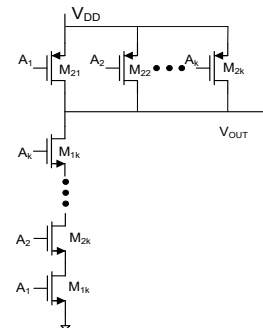
## NOR

$$\frac{C_{IN}}{C_{REF}} = \frac{C_{OX} W_n OD_{HL} L + C_{OX} (3kW_n) OD_{LH} L}{4C_{OX} W_n L} = \frac{OD_{HL} + 3kOD_{LH}}{4}$$



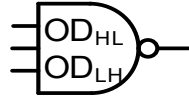
## NAND

$$\frac{C_{IN}}{C_{REF}} = \frac{C_{OX} kW_n OD_{HL} L + C_{OX} (3W_n) OD_{LH} L}{4C_{OX} W_n L} = \frac{k \cdot OD_{HL} + 3OD_{LH}}{4}$$



# Propagation Delay in Multiple-Levels of Logic with Stage Loading

## Asymmetric-sized gates

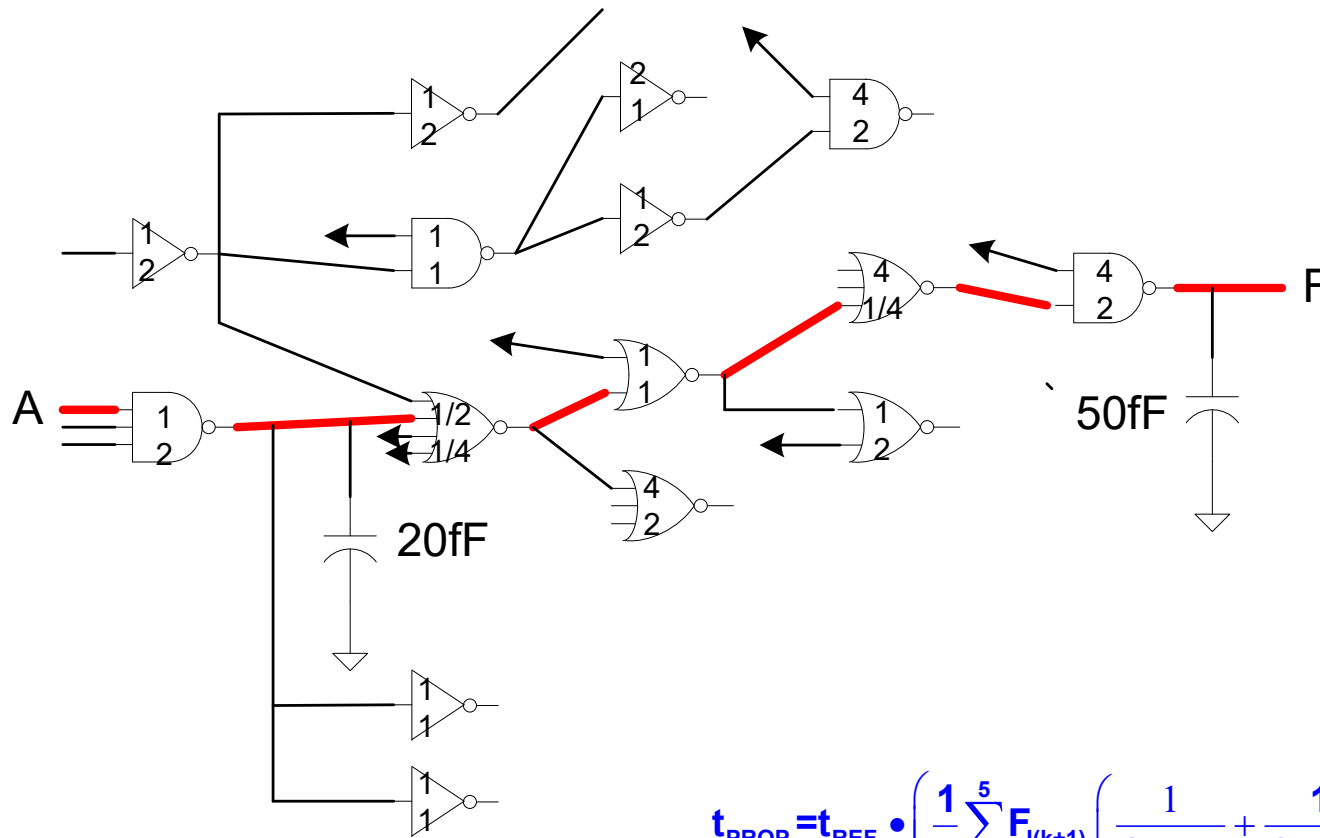


	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD <sub>HL</sub> , OD <sub>LH</sub> )
$C_{IN}/C_{REF}$				
Inverter	1	OD	1/2	$\frac{OD_{HL} + 3 \cdot OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \cdot OD$	1/2	$\frac{OD_{HL} + 3k \cdot OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \cdot OD$	1/2	$\frac{k \cdot OD_{HL} + 3 \cdot OD_{LH}}{4}$
Overdrive				
Inverter				
HL	1	OD	1	OD <sub>HL</sub>
LH	1	OD	1/3	OD <sub>LH</sub>
NOR				
HL	1	OD	1	OD <sub>HL</sub>
LH	1	OD	1/(3k)	OD <sub>LH</sub>
NAND				
HL	1	OD	1/k	OD <sub>HL</sub>
LH	1	OD	1/3	OD <sub>LH</sub>
$t_{PROP}/t_{REF}$	$\sum_{k=1}^n F_{l(k+1)}$	$\sum_{k=1}^n \frac{F_{l(k+1)}}{OD_k}$	$\frac{1}{2} \sum_{k=1}^n F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$	$\frac{1}{2} \sum_{k=1}^n F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$

$$t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

# Propagation Delay in Multiple-Levels of Logic with Stage Loading

## Asymmetric-sized gates

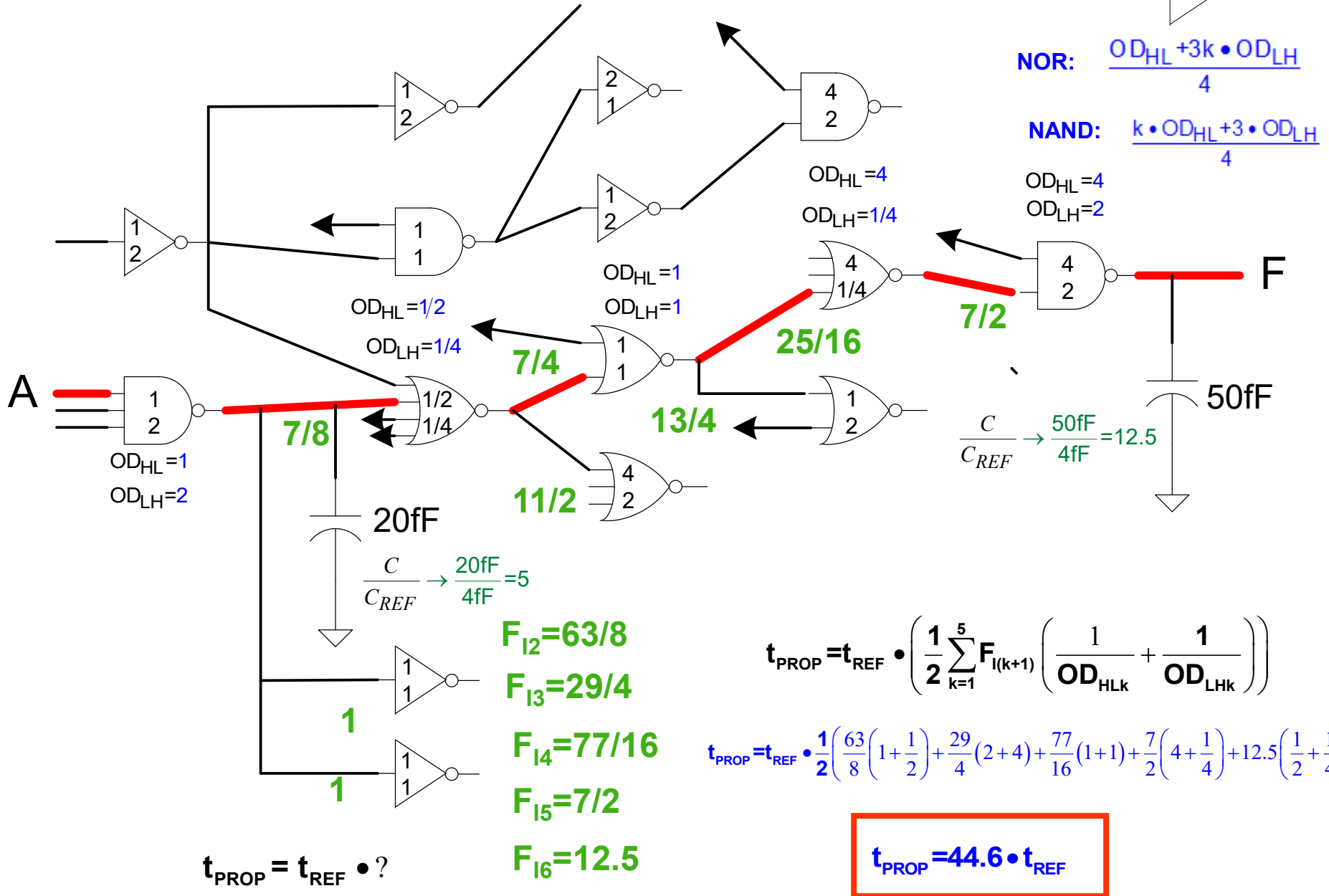
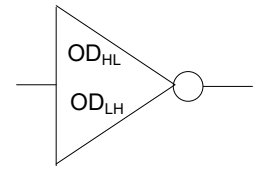


$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^5 F_{l(k+1)} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHK}}} \right) \right)$$

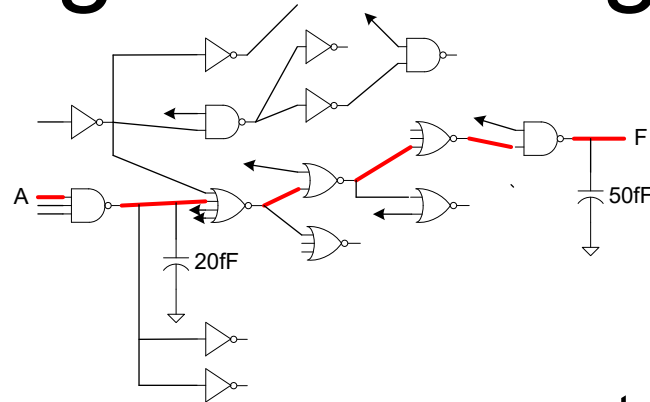


# Asymmetric-sized gates

(Note: This  $C_{OX}$  is somewhat larger than that in the 0.5u ON process)



# Propagation Delay in Multiple-Levels of Logic with Stage Loading



- Equal rise/fall (no overdrive)

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n F_{I_{(k+1)}}$$

- Equal rise/fall with overdrive

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n \frac{F_{I_{(k+1)}}}{\text{OD}_k}$$

- Minimum Sized

$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{I_{(k+1)}} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right)$$

- Asymmetric Overdrive

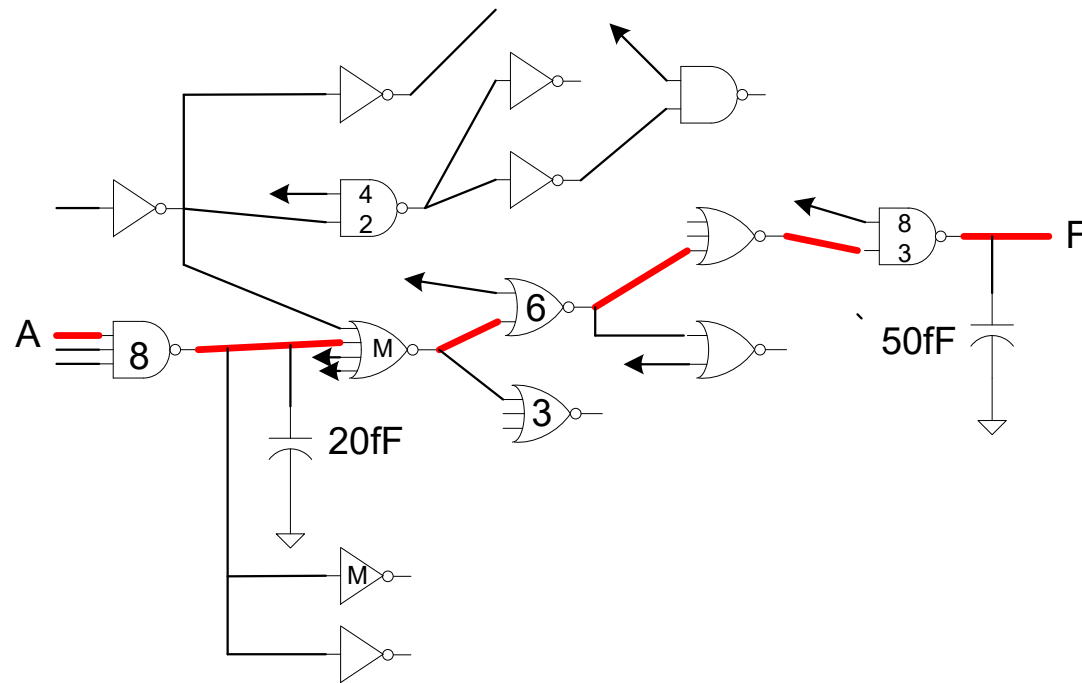
$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{I_{(k+1)}} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right)$$

- ➔ • Combination of equal rise/fall, minimum size and overdrive

$$t_{\text{PROP}} = ?$$

# Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall times and OD*



$$t_{\text{PROP}} = t_{\text{REF}} \bullet ?$$

# Driving Notation

- **Equal rise/fall (no overdrive)**



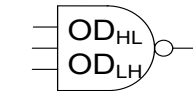
- **Equal rise/fall with overdrive**



- **Minimum Sized**

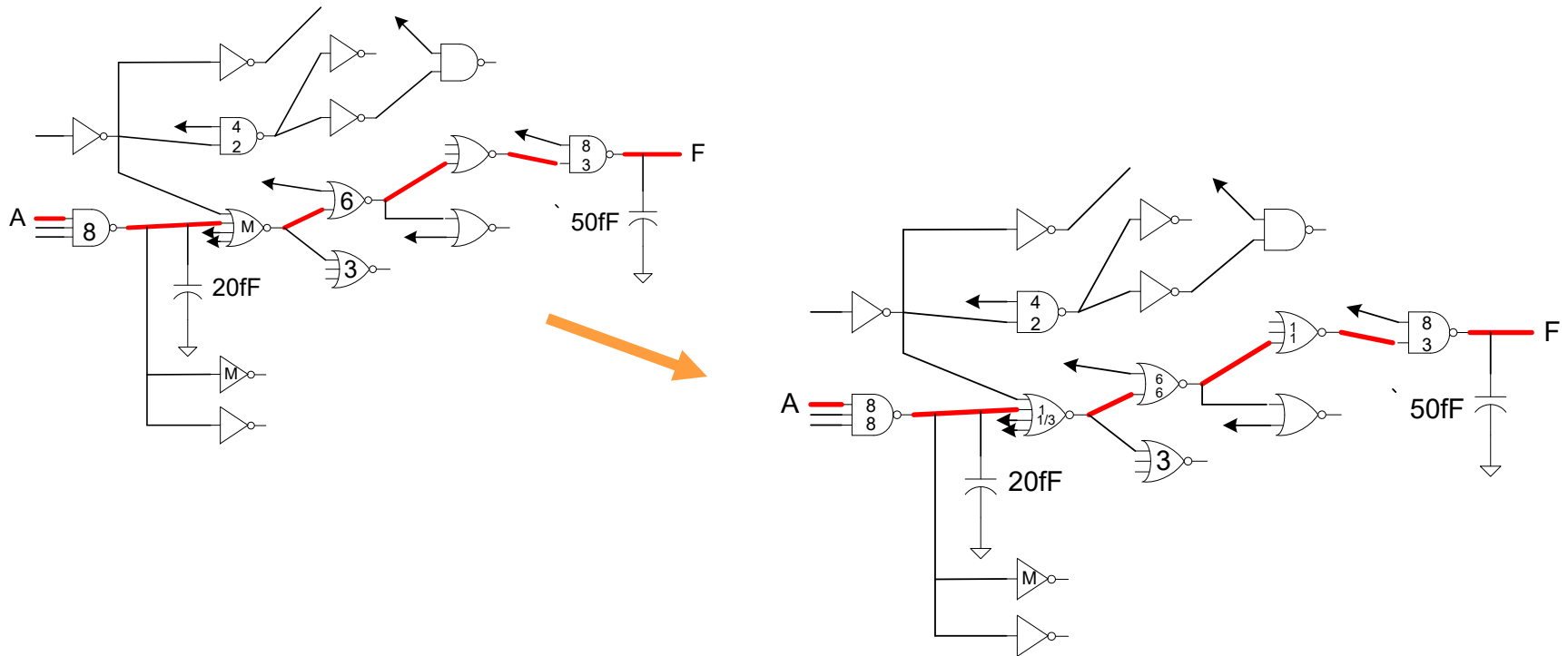


- **Asymmetric Overdrive**



# Propagation Delay in Multiple-Levels of Logic with Stage Loading

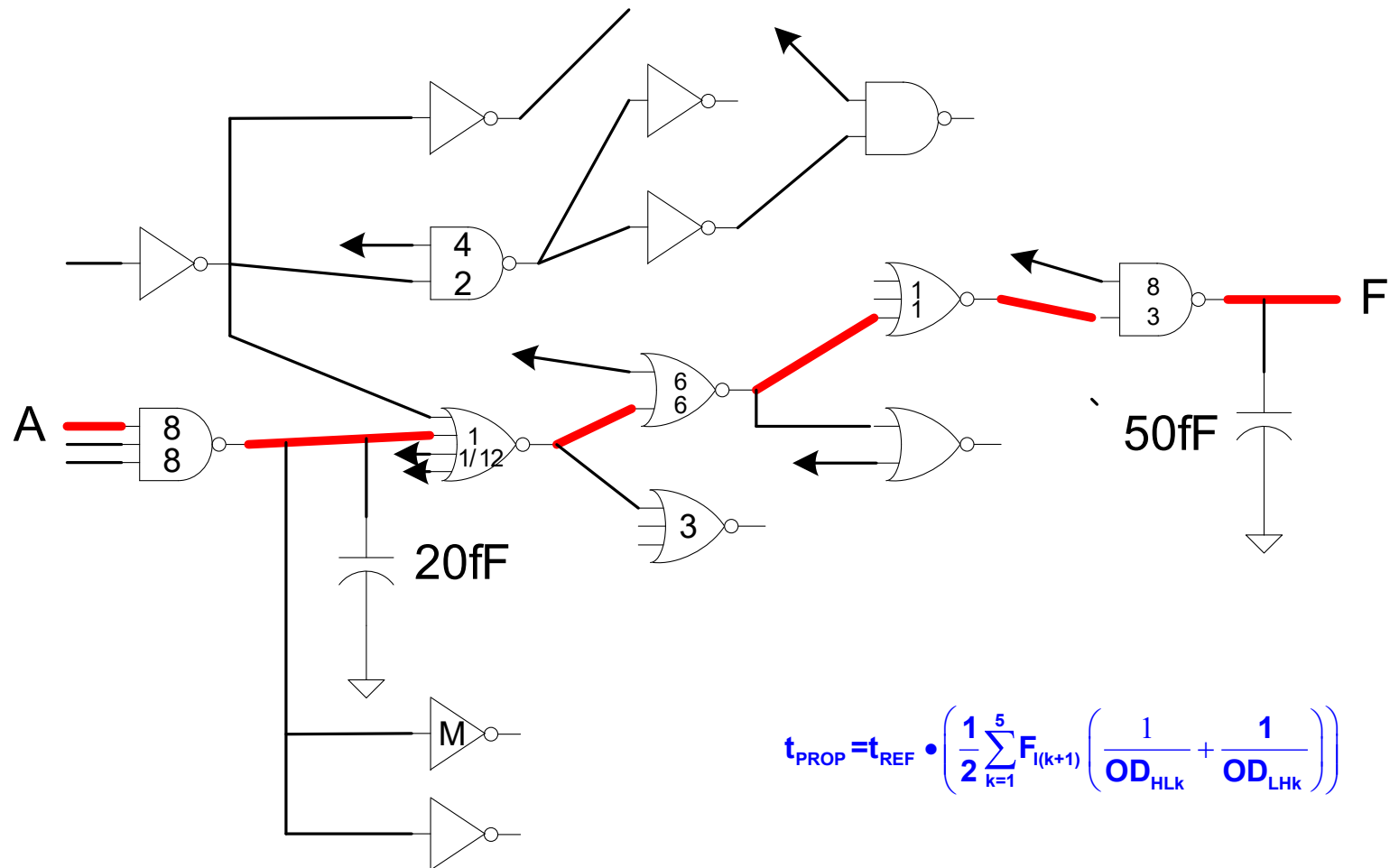
*Mixture of Minimum-sized gates, equal rise/fall gates and OD*



$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^5 F_{l(k+1)} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right)$$

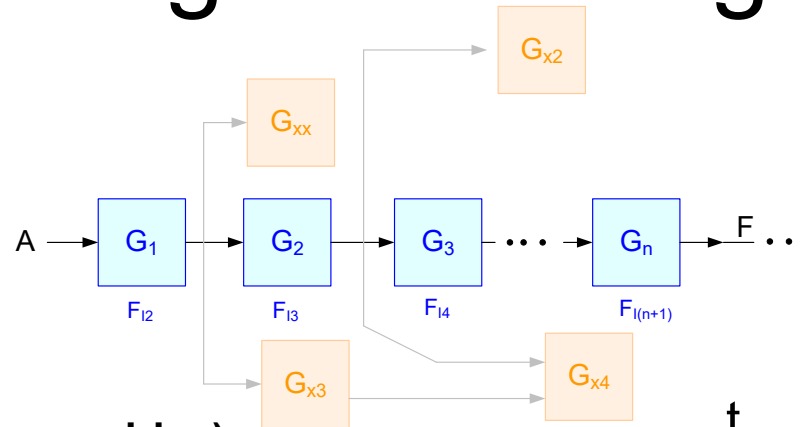
# Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*



$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^5 F_{l(k+1)} \left( \frac{1}{OD_{\text{HLk}}} + \frac{1}{OD_{\text{LHK}}} \right) \right)$$

# Propagation Delay in Multiple-Levels of Logic with Stage Loading



- Equal rise/fall (no overdrive)

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n F_{I(k+1)}$$

- Equal rise/fall with overdrive

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n \frac{F_{I(k+1)}}{\text{OD}_k}$$

- Minimum Sized

$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{I(k+1)} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right)$$




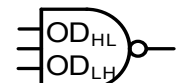
- Asymmetric overdrive

$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{I(k+1)} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right)$$

- Combination of equal rise/fall, minimum size and overdrive

$$t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^n F_{I(k+1)} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right)$$

# Summary: Propagation Delay in Multiple-Levels of Logic with Stage Loading

				
	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD <sub>HL</sub> , OD <sub>LH</sub> )
$C_{IN}/C_{REF}$				
Inverter	1	OD	1/2	$\frac{OD_{HL} + 3 \cdot OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \cdot OD$	1/2	$\frac{OD_{HL} + 3k \cdot OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \cdot OD$	1/2	$\frac{k \cdot OD_{HL} + 3 \cdot OD_{LH}}{4}$
Overdrive				
Inverter				
HL	1	OD	1	OD <sub>HL</sub>
LH	1	OD	1/3	OD <sub>LH</sub>
NOR				
HL	1	OD	1	OD <sub>HL</sub>
LH	1	OD	1/(3k)	OD <sub>LH</sub>
NAND				
HL	1	OD	1/k	OD <sub>HL</sub>
LH	1	OD	1/3	OD <sub>LH</sub>
$t_{PROP}/t_{REF}$	$\sum_{k=1}^n F_{I(k+1)}$	$\sum_{k=1}^n \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2} \sum_{k=1}^n F_{I(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$	$\frac{1}{2} \sum_{k=1}^n F_{I(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$



# Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
      - Logical Effort
    - Elmore Delay
- Sizing of Gates
  - The Reference Inverter

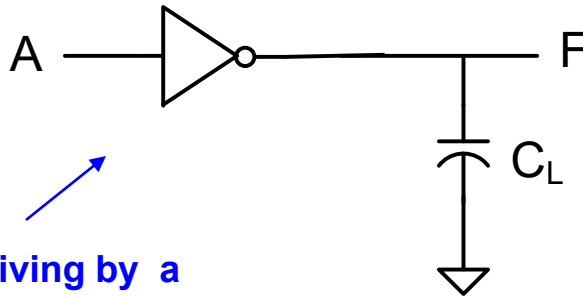
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
  - Other Logic Styles
  - Array Logic
  - Ring Oscillators

→ **done**

→ **partial**

# Driving Large Capacitive Loads

Example



Assume  $C_L = 1000C_{REF}$

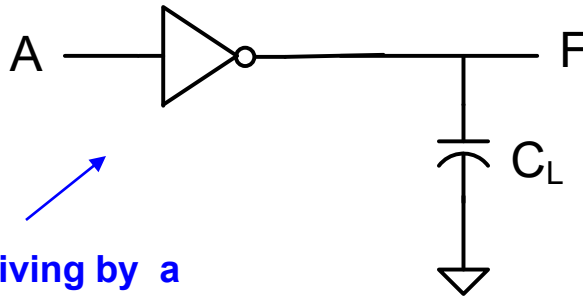
Assume driving by a reference inverter

$t_{PROP} = ?$

In 0.5u proc  $t_{REF} = 20ps$ ,  
 $C_{REF} = 4fF, R_{PDREF} = 2.5K$

# Driving Large Capacitive Loads

## Example



Assume  $C_L = 1000C_{REF}$

Assume driving by a reference inverter

$$t_{PROP} = 1000t_{REF}$$

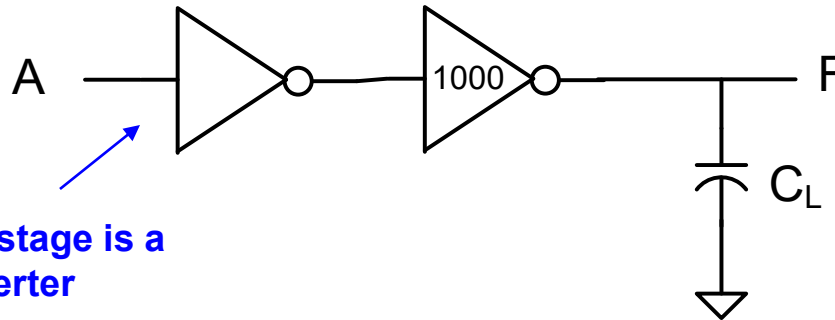
$t_{PROP}$  is too long !

In 0.5u proc  $t_{REF} = 20ps$ ,  
 $C_{REF} = 4fF, R_{PDREF} = 2.5K$

# Driving Large Capacitive Loads

## Example

Assume  $C_L = 1000C_{REF}$



Assume first stage is a reference inverter

$$t_{PROP} = ?$$

$$t_{PROP} = t_{REF} \sum_{k=1}^2 \frac{F_{I(k+1)}}{OD_k}$$

$$t_{PROP} = t_{REF} \left( \frac{1}{1} 1000 + \frac{1}{1000} 1000 \right) = t_{REF} (1000 + 1)$$

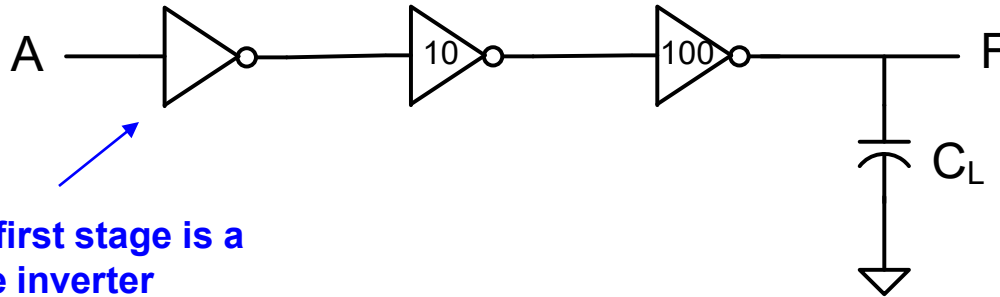
$$t_{PROP} = t_{REF} (1001)$$

**Delay of second inverter is really small but overall delay is even longer than before!**

# Driving Large Capacitive Loads

Example

Assume  $C_L = 1000C_{REF}$



Assume first stage is a reference inverter

$$t_{PROP} = t_{REF} \sum_{k=1}^3 \frac{F_{I(k+1)}}{OD_k}$$

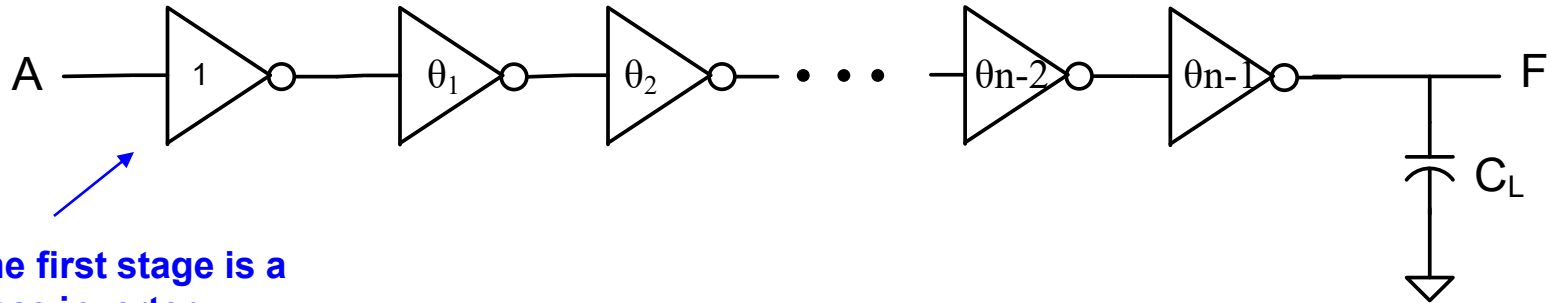
$$t_{PROP} = t_{REF} \left( \frac{1}{1} 10 + \frac{1}{10} 100 + \frac{1}{100} 1000 \right) = t_{REF} (10 + 10 + 10)$$

$$t_{PROP} = 30t_{REF}$$

Dramatic reduction in propagation delay (over a factor of 30!)

What is the fastest way to drive a large capacitive load?

# Optimal Driving of Capacitive Loads



Assume first stage is a reference inverter

Need to determine the number of stages,  $n$ , and the OD factors for each stage to minimize  $t_{\text{PROP}}$ .

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n \frac{F_{I(k+1)}}{\text{OD}_k} \longrightarrow t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n \frac{\theta_k}{\theta_{k-1}}$$

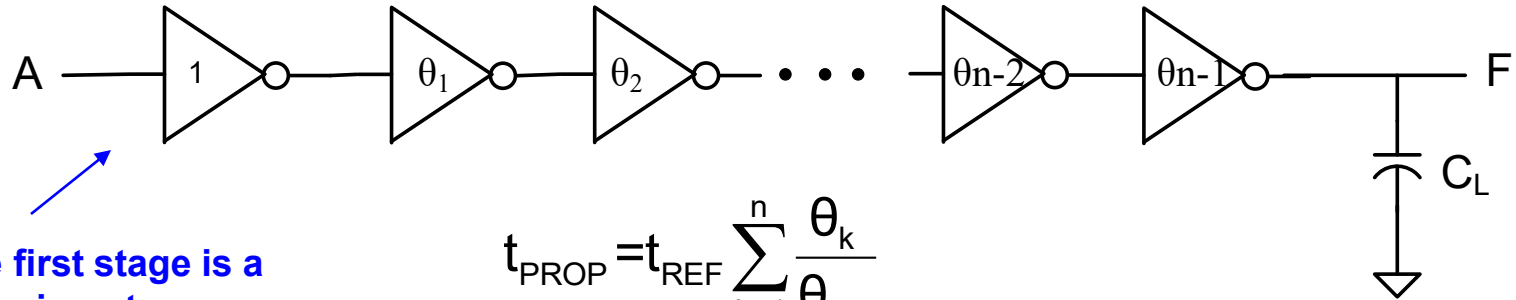
$$\text{where } \theta_0 = 1, \theta_n = C_L / C_{\text{REF}}$$

This becomes an  $n$ -parameter optimization (minimization) problem !

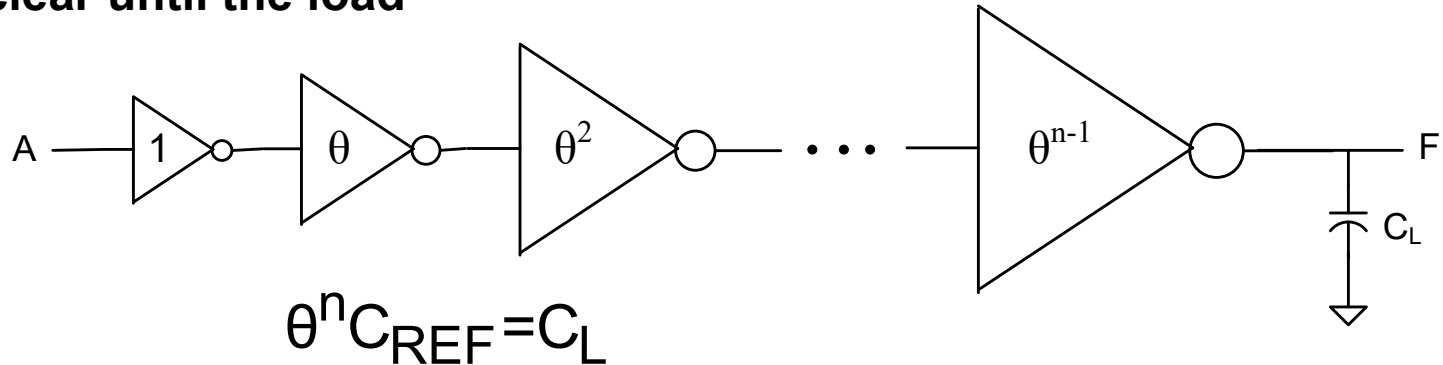
Unknown parameters:  $\{\theta_1, \theta_2, \dots, \theta_{n-1}, n\}$

**An  $n$ -parameter nonlinear optimization problem is generally difficult !!!!**

# Optimal Driving of Capacitive Loads



**Order reduction strategy : Assume overdrive of stages increases by the same factor clear until the load**



**This becomes a 2-parameter optimization (minimization) problem !**

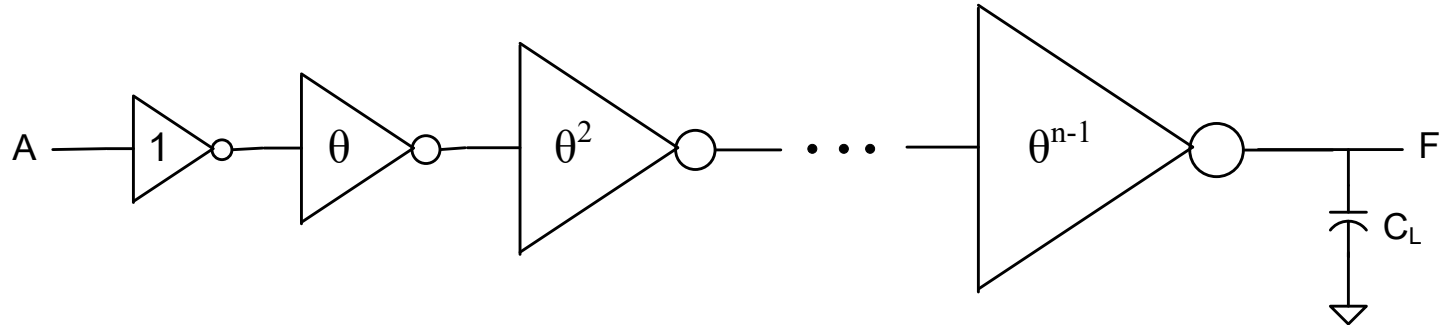
**Unknown parameters:  $\{\theta, n\}$**

**One constraint :  $\theta^n C_{\text{REF}} = C_L$**



**One degree of freedom**

# Optimal Driving of Capacitive Loads



$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n \frac{\theta_k}{\theta_{k-1}}$$



$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n \frac{\theta^k}{\theta^{k-1}}$$

$$t_{\text{PROP}} = t_{\text{REF}} n\theta$$

$$\theta^n C_{\text{REF}} = C_L$$

or

$$F|_L = \theta^n$$

$$\left. \begin{array}{l} t_{\text{PROP}} = t_{\text{REF}} n\theta \\ \theta^n C_{\text{REF}} = C_L \end{array} \right\}$$

Unknown parameters:  $\{\theta, n\}$

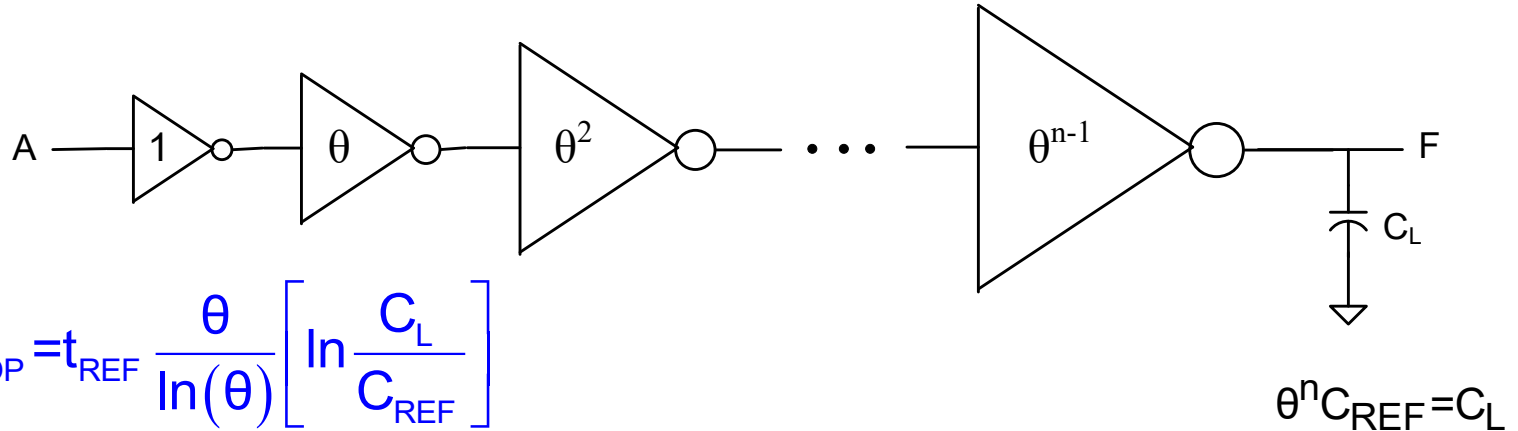
$$\theta^n C_{\text{REF}} = C_L \longrightarrow n = \frac{1}{\ln(\theta)} \ln\left(\frac{C_L}{C_{\text{REF}}}\right)$$

Thus obtain an expression for  $t_{\text{PROP}}$  in terms of only  $\theta$

$$t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right]$$



# Optimal Driving of Capacitive Loads



$$t_{PROP} = t_{REF} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{REF}} \right]$$

It suffices to minimize the function

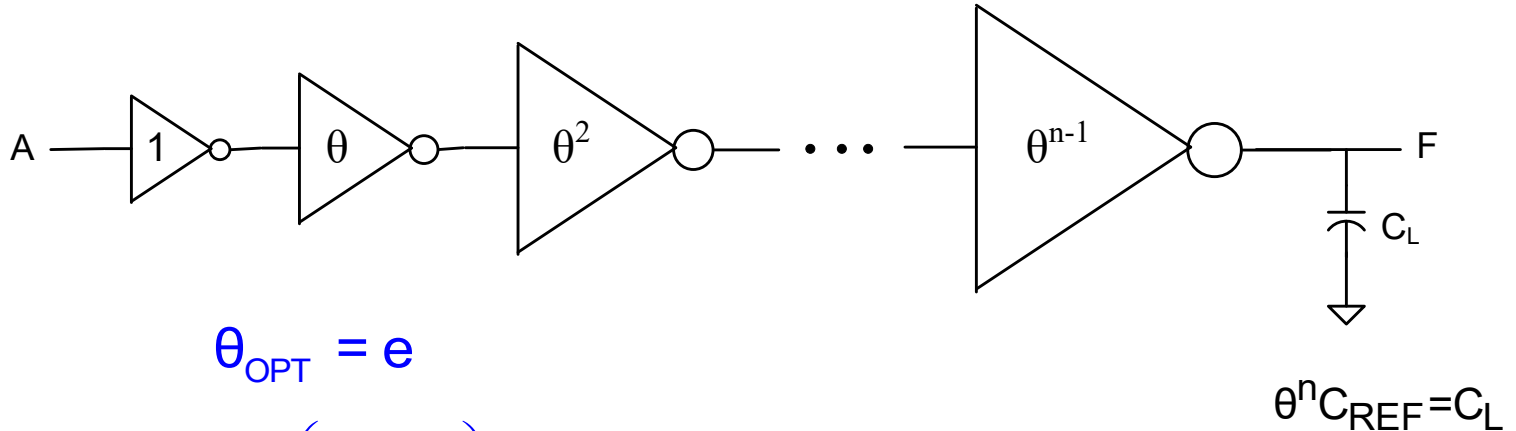
$$f(\theta) = \frac{\theta}{\ln(\theta)}$$

$$\frac{df}{d\theta} = \frac{\ln(\theta) - \theta \cdot \left( \frac{1}{\theta} \right)}{(\ln(\theta))^2} = 0$$

$$\ln(\theta) - 1 = 0 \quad \rightarrow \quad \theta = e$$

$$n = \frac{1}{\ln(\theta)} \ln \left( \frac{C_L}{C_{REF}} \right) \quad \rightarrow \quad n = \ln \left( \frac{C_L}{C_{REF}} \right) = \ln(FI_L)$$

# Optimal Driving of Capacitive Loads



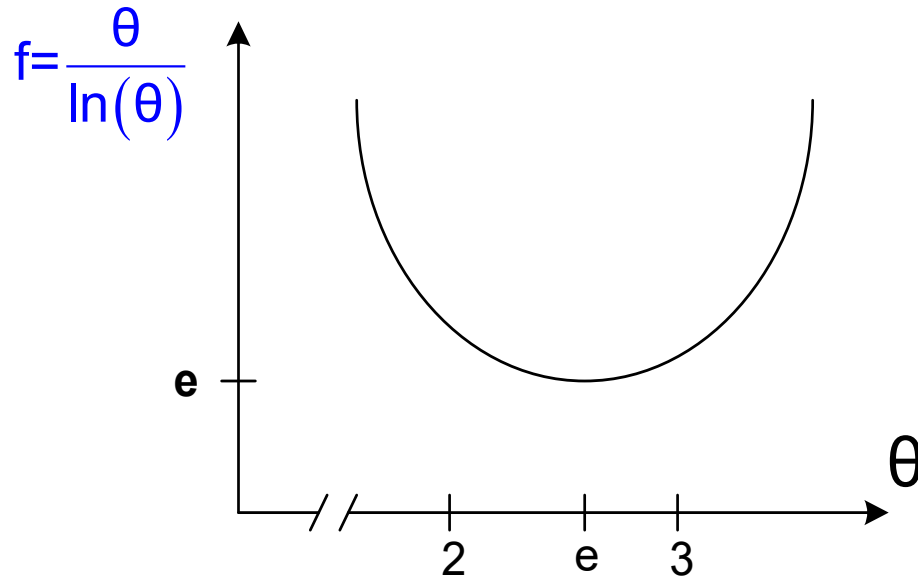
$$t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right]$$

$$t_{\text{PROP}} = t_{\text{REF}} e \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] = \text{net}_{\text{REF}}$$

- Since  $\theta_{\text{OPT}} = e$  is an irrational number, snap-size limitations in layout tools make it impossible to use the optimal scaling factor (even if  $n$  comes out to be an integer).
- Need a practical solution

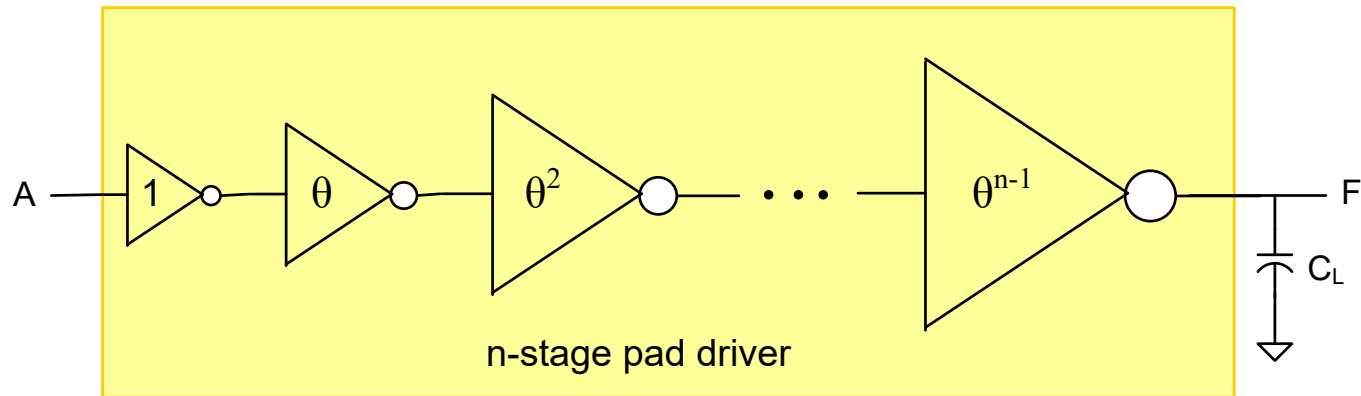
# Optimal Driving of Capacitive Loads

A practical solution



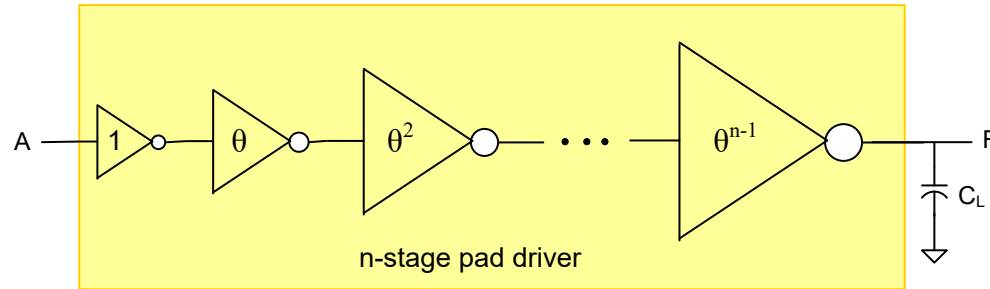
- minimum at  $\theta=e$  but shallow inflection point for  $2<\theta<3$
- practically pick  $\theta=2$ ,  $\theta=2.5$ , or  $\theta=3$
- since optimization may provide non-integer for  $n$ , must pick close integer

# Optimal Driving of Capacitive Loads



- **Often termed a pad driver**
- **Often used to drive large internal busses as well**
- **Generally included in standard cells or in cell library**
- **Device sizes can become very large**
- **Odd number of stages will cause signal inversion but usually not a problem**

# Optimal Driving of Capacitive Loads



**Example:** Design a pad driver for driving a load capacitance of 10pF with equal rise/fall times, determine  $t_{PROP}$  for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc  $t_{REF}=20ps$ ,  
 $C_{REF}=4fF, R_{PDREF}=2.5K$

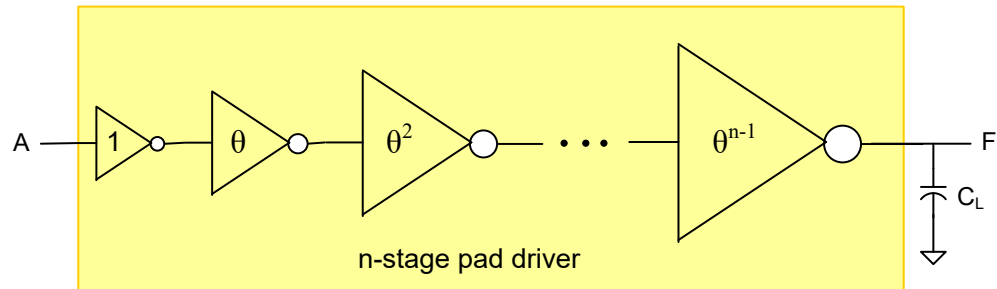
$FIL=2500$

$$n_{OPT} = \ln\left(\frac{C_L}{C_{REF}}\right) = \ln\left(\frac{10pF}{4fF}\right) = \ln(2500) = 7.8$$

**Select  $n=8, \theta=2.5$**

$$W_{nk} = 2.5^{k-1} \cdot W_{REF}, \quad W_{pk} = 3 \cdot 2.5^{k-1} \cdot W_{REF}$$

# Optimal Driving of Capacitive Loads



**Example:** Design a pad driver for driving a load capacitance of 10pF with equal rise/fall times, determine  $t_{PROP}$  for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc  $t_{REF}=20ps$ ,  
 $C_{REF}=4fF, R_{PDREF}=2.5K$

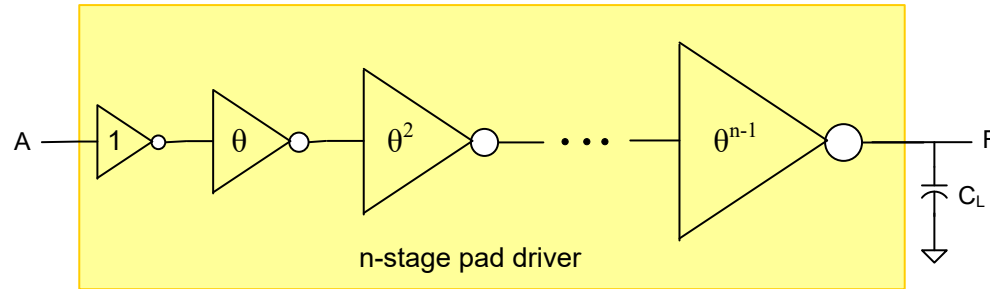
For  $\theta = 2.5$ ,  $n=8$   $W_{REF}=W_{MIN}$   
 $W_{nk}=2.5^{k-1} \cdot W_{REF}$ ,  $W_{pk} = 3 \cdot 2.5^{k-1} \cdot W_{REF}$

$$L_n = L_p = L_{MIN}$$

k	n-channel	p-channel
1	1 $W_{MIN}$	3 $W_{MIN}$
2	2.5 $W_{MIN}$	7.5 $W_{MIN}$
3	6.25 $W_{MIN}$	18.75 $W_{MIN}$
4	15.6 $W_{MIN}$	46.9 $W_{MIN}$
5	39.1 $W_{MIN}$	117.2 $W_{MIN}$
6	97.7 $W_{MIN}$	293.0 $W_{MIN}$
7	244.1 $W_{MIN}$	732.4 $W_{MIN}$
8	610.4 $W_{MIN}$	1831.1 $W_{MIN}$

**Note devices in last stage are very large !**

# Optimal Driving of Capacitive Loads



**Example:** Design a pad driver for driving a load capacitance of 10pF with equal rise/fall times, determine  $t_{PROP}$  for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc  $t_{REF}=20ps$ ,  
 $C_{REF}=4fF, R_{PDREF}=2.5K$

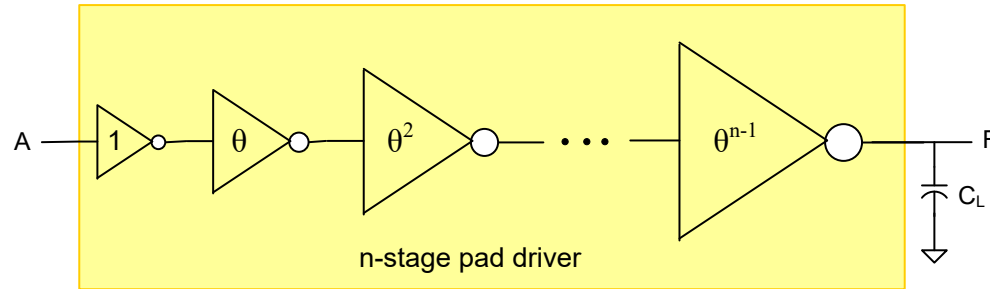
$$W_{nk} = 2.5^{k-1} \cdot W_{REF}, \quad W_{pk} = 3 \cdot 2.5^{k-1} \cdot W_{REF}$$

$$t_{PROP} \cong n\theta t_{REF} = 8 \cdot 2.5 \cdot t_{REF} = 20t_{REF}$$

**More accurately:**

$$t_{PROP} = t_{REF} \left( \sum_{k=1}^7 \theta + \frac{1}{\theta^7} \frac{C_L}{C_{REF}} \right) = t_{REF} \left( 17.5 + \frac{1}{610} 2500 \right) = 21.6t_{REF}$$

# Optimal Driving of Capacitive Loads



**More accurately:**

$$t_{\text{PROP}} = t_{\text{REF}} \left( \sum_{k=1}^7 \theta + \frac{1}{\theta^7} \frac{C_L}{C_{\text{REF}}} \right) = t_{\text{REF}} \left( 17.5 + \frac{1}{610} 2500 \right) = 21.6 t_{\text{REF}}$$

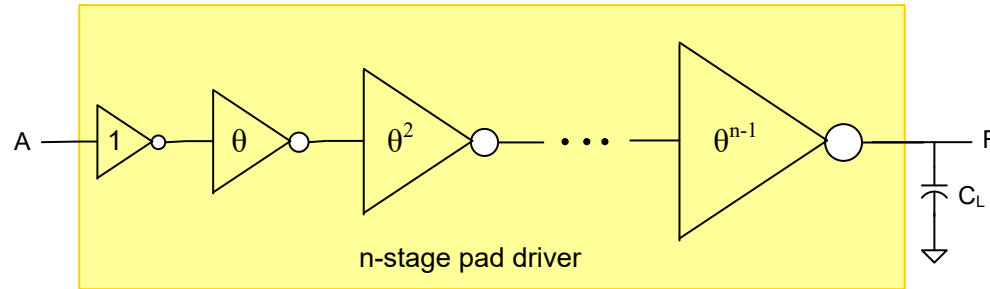
**Possible modest improvement for determining n and  $\theta$  after determining  $n_{\text{opt}}$ :**

Consider all possible combinations of  $\theta$  in  $\{ 2, 2.5, 3 \}$  and  $n$  in  $\{ \text{INT}(n_{\text{opt}}), 1 + \text{INT}(n_{\text{opt}}) \}$

$$t_{\text{PROP}}(\theta, n) = t_{\text{REF}} \left( \sum_{k=1}^{n-1} \theta + \frac{1}{\theta^{n-1}} \frac{C_L}{C_{\text{REF}}} \right) = t_{\text{REF}} \left( (n-1)\theta + \frac{1}{\theta^{n-1}} F_{I_L} \right)$$



# Optimal Driving of Capacitive Loads



**Example:** Design a pad driver for driving a load capacitance of 10pF with equal rise/fall times, determine  $t_{PROP}$  for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc  $t_{REF}=20ps$ ,  
 $C_{REF}=4fF, R_{PDREF}=2.5K$

$$W_{nk} = 2.5^{k-1} \cdot W_{REF}, \quad W_{pk} = 3 \cdot 2.5^{k-1} \cdot W_{REF}$$

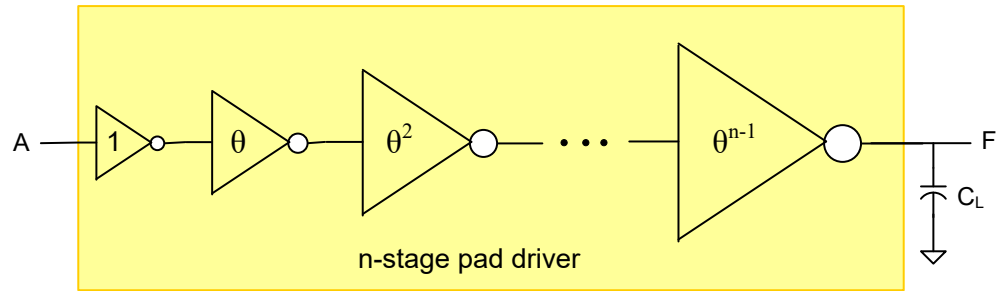
**If driven directly with the minimum-sized reference inverter**

$$t_{PROP} = t_{REF} \frac{C_L}{C_{REF}} = 2500 t_{REF}$$

**Note an improvement in speed by a factor of approximately**

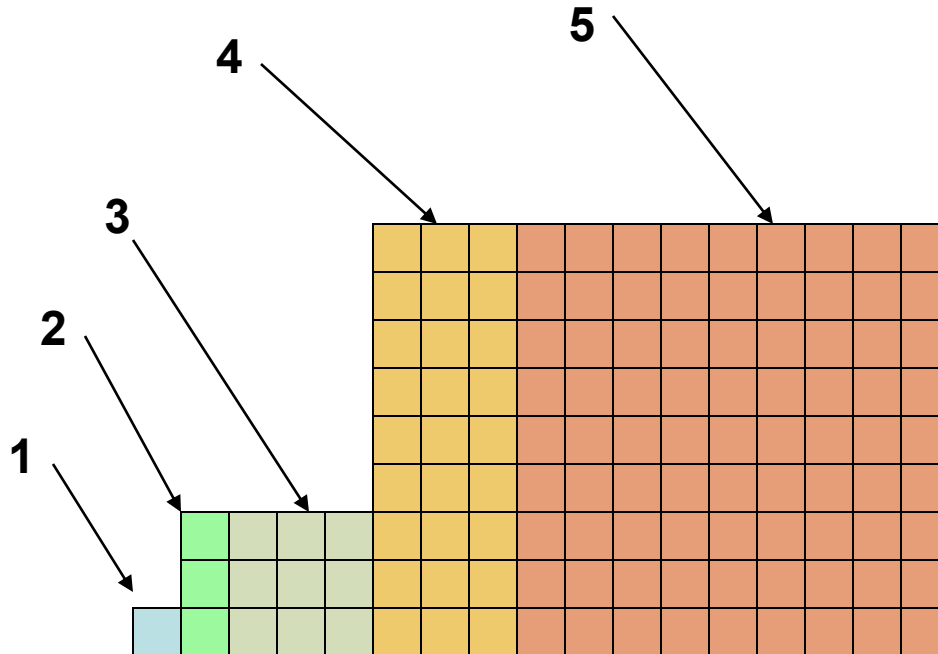
$$r = \frac{2500}{20} = 125$$

# Pad Driver Size Implications



Consider a 7-stage pad driver and assume  $\theta = 3$

 : Area of Ref Inverter

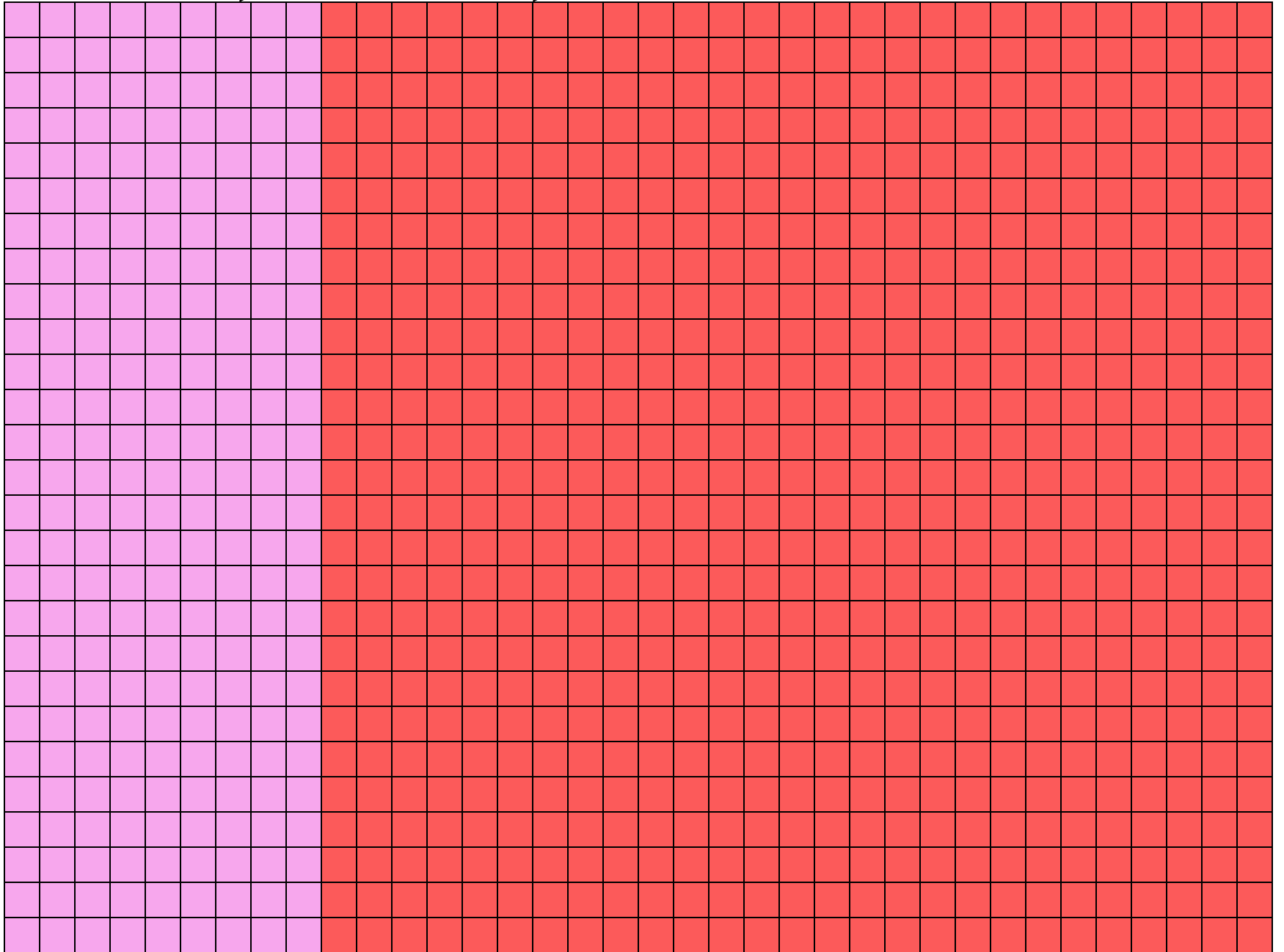




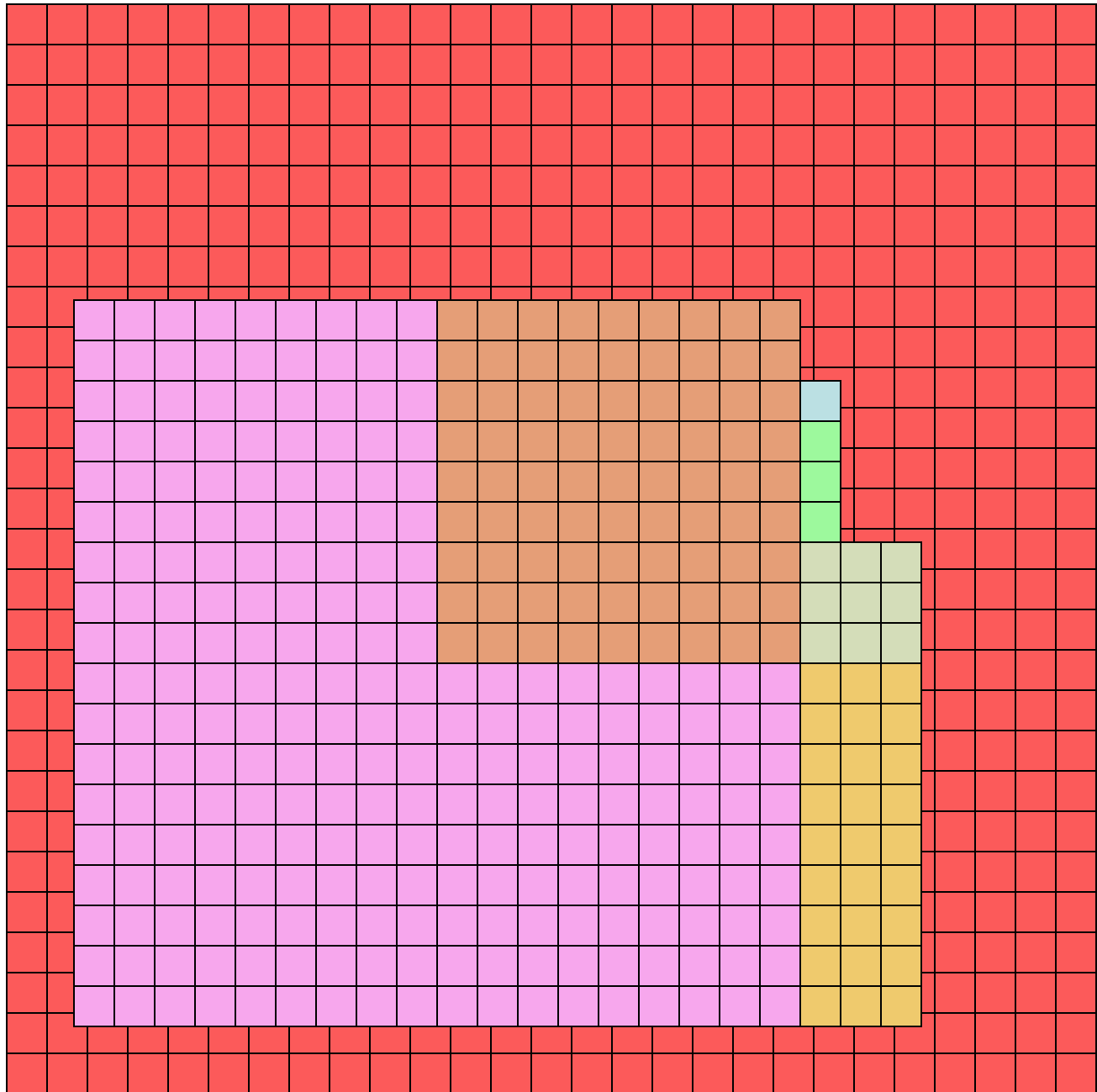
6



7



**Area of Last Stage Larger than that of all previous stages combined!**



# Propagation Delay in “Logic Effort” approach

(Discussed in Chapter 4 of Text but definitions are not rigorous)

## Logical effort

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From Wikipedia, the free encyclopedia **(Dec 8, 2021)**

The method of **logical effort**, a term coined by [Ivan Sutherland](#) and [Bob Sproull](#) in 1991, is a straightforward technique used to [estimate delay](#) in a [CMOS](#) circuit. Used properly, it can aid in selection of gates for a given function (including the number of stages necessary) and sizing gates to achieve the minimum delay possible for a circuit.

# Propagation Delay in “Logic Effort” approach

(Discussed in Chapter 4 of Text but definitions are not rigorous)

Propagation delay for equal rise/fall gates was derived to be

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n \frac{F_{l(k+1)}}{OD_k}$$

Delay calculations with “logical effort” approach

Logical effort delay approach:

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n f_k$$

( $t_{\text{REF}}$  scaling factor not explicitly stated in W\_H textbook. As defined in W\_H,  $f_k$  is dimensionless)

where  $f_k$  is the “effort delay” of stage  $k$

$$f_k = g_k h_k$$

$g_k$  = logical effort

$h_k$  = electrical effort

# Propagation Delay in “Logic Effort” approach

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n f_k \quad f_k = g_k h_k$$

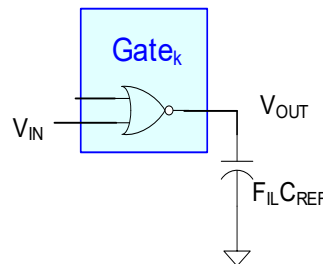
$f_k$  = “effort delay” of stage  $k$

$g_k$  = logical effort

$h_k$  = electrical effort

**Logic Effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current**

**Electrical Effort is the ratio of the gate load capacitance to the input capacitance of a gate**

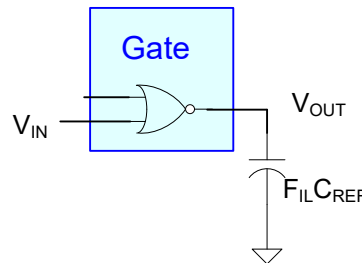


# Propagation Delay in “Logic Effort” approach

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n f_k \quad f_k = g_k h_k$$

**Logic Effort (g)** is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current

**Electrical Effort (h)** is the ratio of the gate load capacitance to the input capacitance of a gate



$$g_k = \frac{C_{\text{IN}_k}}{C_{\text{REF}} \cdot \text{OD}_k}$$

$$h_k = \frac{C_{\text{REF}} \cdot F_{\text{I}_{k+1}}}{C_{\text{IN}_k}}$$



# Propagation Delay in “Logic Effort” approach

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n f_k \quad f_k = g_k h_k$$

$$g_k = \frac{C_{\text{IN}_k}}{C_{\text{REF}} \cdot \text{OD}_k} \quad h_k = \frac{C_{\text{REF}} \cdot F_{\text{I}(k+1)}}{C_{\text{IN}_k}}$$

$$f_k = \left( \frac{\cancel{C_{\text{IN}_k}}}{\cancel{C_{\text{REF}} \cdot \text{OD}_k}} \right) \left( \frac{\cancel{C_{\text{REF}} \cdot F_{\text{I}(k+1)}}}{\cancel{C_{\text{IN}_k}}} \right)$$

$$f_k = \frac{F_{\text{I}(k+1)}}{\text{OD}_k}$$

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n f_k = t_{\text{REF}} \sum_{k=1}^n g_k h_k = t_{\text{REF}} \sum_{k=1}^n \frac{F_{\text{I}(k+1)}}{\text{OD}_k}$$

# Propagation Delay in “Logic Effort” approach

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^n f_k = t_{\text{REF}} \sum_{k=1}^n g_k h_k = t_{\text{REF}} \sum_{k=1}^n \frac{F_{l(k+1)}}{OD_k}$$

- **Note this expression is identical to what we have derived previously**  
( $t_{\text{REF}}$  scaling factor not included in W\_H text)
- **Probably more tedious to use the “Logical Effort” approach**
- **Extensions to asymmetric overdrive factors may not be trivial**
- **Extensions to include parasitics may be tedious as well**
- **Logical Effort is widely used throughout the industry**



**Stay Safe and Stay Healthy !**

**End of Lecture 42**